REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 9-11, 14, 15, 24-46, and 48-53 are pending in this application. Claims 1-8, 12, 13, 16-23, and 47 have all been previously canceled without prejudice or disclaimer. Claims 9, 25, 27-29, and 36 have been amended to correct a typographical error without the introduction of any new matter.

The outstanding Official Action presents an objection to Claims 9, 25-29, and 36 as inserting new matter, a rejection of Claims 9-11, 14, 15, 25-46, and 48-53 under the first paragraph of 35 U.S.C. § 112, a rejection of Claims 9-11, 14, 15, 24-29, 34-45, and 48-53 under 35 U.S.C. § 103(a) as being unpatentable over Rogers et al, (U.S. patent No. 4,571,819, Rogers) in view of Lee et al (U.S. Patent No. 4,952,524, Lee), and a rejection of Claims 30-33 and 46 as being unpatentable over Rogers in view of Lee and in further view of Dash et al. (U.S. Patent No. 5,173,439, Dash).

The objection based upon new matter made at page 2 of the outstanding Action as to the language in Claims 9, 25-29, and 36 that was added by amendment is clearly improper. See In re Rasmussen, 211 USPQ 323 (CCPA 1981); MPEP §706.03(o); MPEP §2163.01; and MPEP §2163.06, all as noted in the previous response.

Turning first to MPEP §706.03(o) (Rev. 2. May 2004), this section notes that "[i]f new matter is added only to a claim, an objection using [Form Paragraph 7.28] should not be made, but the claim should be rejected using Form Paragraph 7.31.01" (emphasis added). MPEP §2163.01 (Rev. 2. May 2004) also notes that if it is determined "that the claimed subject matter is not supported [described] in an application as filed," the claim is to be rejected using the written description requirement of the first paragraph of 35 U.S.C. §112,

not "rejected or objected to on the ground of new matter." The reason given in this section is that the above-noted Rasmussen decision limits any 35 U.S.C. §132 new matter objection to be "an objection to amendments to the abstract, specification or drawings." Further note that MPEP §2163.06 (I) (Rev. 2. May 2004) repeats these instructions and again cites the Rasmussen decision.

MPEP §2163.06 (II) (Rev. 2, May 2004) further notes that that even if an objection as to new matter is made along with a corresponding rejection using the written description requirement of the first paragraph of 35 U.S.C. §112, these issues are to be decided on appeal to the Board. This section clearly precludes the requirement in the outstanding Action for the deletion of the objected to subject matter, as this would infringe on Applicants' right to appeal to the Board for review of the propriety of the objection along with that of the corresponding rejection.

Accordingly, the withdrawal of this clearly improper and un-authorized objection to Claims 9, 25-29, and 36 is respectfully submitted to be in order as is withdrawal of the requirement to cancel the subject matter objected to as being drawn to new matter from these claims in response to the outstanding Action.

Turning to the asserted lack of a written description to support the objected to subject matter of Claims 9-11, 14, 15, 24-46, and 48-53, it is noted that page 3 of the outstanding Action again relies on the MPEP §2173.05(i) and a statement therein (requiring that any negative limitation must "have basis in the original disclosure") incorrectly asserted to be from the cited Schecter decision.

However, and as noted in the last response, MPEP §2173.05(i) merely points out that the Schecter case represents older decisions critical of negative limitations in terms of violating the second paragraph of 35 U.S.C. §112. This section goes on to note that the

current view is that a negative limitation can be used because such a limitation does not inherently violate the second paragraph of 35 U.S.C. §112. While this section does note the requirement for a "basis in the original disclosure" for a negative limitation, it does not state that this is a requirement arising from the Schecter case.

In any event, and as further noted in the last response, this requirement for a "basis in the original disclosure" is not a requirement that there must be literal support present in the specification before a negative limitation can be used in a claim. In this regard, this section specifically cautions examiners that "a lack of literal basis in the specification may not be sufficient to establish a *prima facie* case for lack of descriptive support" (emphasis added).

This caution is in agreement with controlling court decisions noted in the last response that set forth that the PTO may not interpret the written description requirement to require literal (exact word) support in the specification. See, e.g., Martin v. Johnson 172 USPQ 391, 395 (CCPA 1972) (stating "the description need not be in ipsis verbis [i.e. "in the same words"] to be sufficient"). The PTO further acknowledges this controlling court precedent in MPEP §2163.02 that notes that "[t]he subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement" (col. 1 on page 2100-178 of Rev. 2, May, 2004).

Page 14 of the outstanding Action appears to misconstrue this point to be an assertion by Applicants that the lack of a positive recital of the presence of a dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide in the specification is being urged to be **ALONE** a basis for claiming this lack of a melting-temperature-lowering dopant of boron or phosphorus in the silicon oxide film. Instead of suggesting this, the last response pointed out that the statement of page 3, lines 32-36, of the original specification ("....., it is difficult in the existing state to obtain high purity organic silicon source because

of limitation in a material refining technique for the organic silicon source") and the clear teaching of this statement to the worker of ordinary skill in the art familiar with the meaning of "high purity" is one (but not the only) disclosure that points to providing a highly pure silicon oxide film from the high purity source. In this respect, those of ordinary skill in the art would clearly understand that the language "high purity" has a meaning that precludes the presence of impurities, like dopants of boron or phosphorus.

Moreover, it is submitted that workers of ordinary skill in the art would further know that TEOS is an acronym used to indicate a type of source (tetraethylorthossilicate) of known composition ($Si(OC_2H_5)_4$) as noted at page 3, lines 11-14 of the specification, for example. Those familiar with chemistry, as the worker of ordinary skill must be, would understand that the very name (tetraethylorthossilicate) and its known composition ($Si(OC_2H_5)_4$) clearly indicate the absence of any boron or phosphorus. Similarly, the chemical definitions presented at page 9, lines 20-26 of this organic silicon material and the others suitable for the "organic silicon based CVD method" for producing the silicon oxide films would be understood by the artisan to contain no boron and/or phosphorus.

As further noted in the last Action, the acronym "BPTEOS" is used by the artisan to indicate the presence of these dopants of boron or phosphorus or the material is referred to as being "doped TEOS." The worker of ordinary skill in the art would, thus, understand that there is a distinction as between "TEOS" and "BPTEOS." Note, for example, the abstract and col. 4, lines 28-38 in Lee, relied upon to reject the claims based upon obviousness, that disclose the understanding of the artisan that phosphorus and boron dopants are present in "BPTEOS" and not in "TEOS." Note the further acronym "PTEOS" (discussed at col. 4, lines 65-68) is used by the artisan when just phosphorus dopant is present.

It is not clear if the PTO is simply ignoring the meaning to the artisan of the specification requirement for a "high purity organic silicon source" and the difference to the artisan between "TEOS," PTEOS," and "BPTEOS" established by Lee, or if the PTO needs more evidence of the artisans understanding that "TEOS" CVD processing is employed to produce SiO_2 films without boron or phosphorus being present. If the PTO is simply seeking added evidence of the use and meaning of "TEOS," Applicants submit herewith Documents 1, 13, 16, 18, 20, and 24 that are included as part of the attached "LISTING AND COMMENT ON DOCUMENTARY EVIDENCE that precedes the attached numbered documents 1-24 and gives a brief synopses of the content of each document and the reason it is cited as evidence that the present application including an adequate written description of the invention under the first paragraph of 35 U.S.C. §112 and or why the PTO assertions of inherent results of heating are without merit, as well as identifying documents 1-24 by author, title, date, and page(s).

While the disclosure also indicates that the Spin-On-Glass (SOG) method is an alternative to the claimed "CVD method using an electrically inert organic silicon source," see page 6, lines 5-8, and page 23, lines 13-19, Document 17 indicates that SOG methods also inherently produce oxides without boron or phosphorus dopants.

In any event, it is sufficient that the disclosure teaches the use of the above-noted films formed using the claimed CVD method and organic based silicon source materials disclosed at page 9, lines 20-26 in terms of chemical formulas that do not include either boron or phosphorus. Those familiar with chemical formulas, like the worker of ordinary skill in the art, would recognize that if either boron or phosphorus were included, the formulas given would include the chemical symbol for boron or phosphorus. As the chemical formulas presented in the specification include no chemical symbol indicating any

boron or phosphorus is included with the organic silicon source materials to be used with the CVD method is if they are provided from some other source. However, no such source of boron or phosphorus is disclosed.

Furthermore, the disclosure of other suitable materials possibly being included in the formed oxide does not mean that they must be included or that they would produce the same results the inclusion of boron and/or phosphorus would. In addition, in terms of a CVD method using organic silicon source with a silicon hydrogen compound such as SiH_4, or silicon chloride such as $SiCl_4$, there is no disclosure that dopants reducing melting temperature, like boron and phosphorus, are present or result after the method is performed.

In addition, Fig. 7B of this application shows clearly the relationships between the etching rates of the claimed non-doped oxide film and annealing temperature while Fig. 7A shows the relationship of ring structures and dislocation suppression to annealing temperature for the oxide film formed using such an organic silicon source-CVD method. If the oxide films had been doped with boron or phosphorus, the relationships between the etching rates and annealing temperature would show different curves and the films would melt in the range of 950 to 1150 degree C as taught by Rogers (see col. 6, lines 26-29) relied upon in the outstanding Action to reject all of the pending claims.

In this regard, the annealing point of any glass substance is well understood to relate to particular viscosity conditions vastly different from melting viscosities. See the attached copy of pages 572-73 of the "Kirk-Othmer Encclopedia of Chemical Technology" (1994) with regard to the viscosity points labeled on the right hand vertical axis of Fig. 6 and the discussion of melting viscosities at page 573, lines 16-18. The apparent reading of "annealing temperature" for oxides formed from the disclosed and claimed organic silicon sources by a CVD method of the present application as being the same thing and having the

same inherent results as subjecting the Rogers doped glass layer to its melting temperature is clearly without basis in fact here or in the below noted prior art based rejections.

Further in this regard, if the disclosed oxide films formed by a CVD method using an organic silicon source were doped with boron or phosphorus in some manner clearly not disclosed in the present application, then the Raman spectra shown in Figs. 6A and 6B of this application would indicate the presence of boron or phosphorus by peaks in the illustrated curves at 670 cm^{-1} and at 520 cm^{-1}. Note again the **Journal of Non-Crystalline Solids** article attached to the Amendment filed November 7, 2002, and its showing that if a silicon oxide film contains boron, the Raman spectra should have a peak at 670 cm^{-1} (See Fig.3 and table 3 of **Journal of Non-Crystalline Solids**). Further, if the measured silicon oxide film had contained phosphorus, the Raman spectra should have a peak at 520 cm^{-1} (See Fig.4 and table 4 of **Journal of Non-Crystalline Solids**). As no peak at 670 cm^{-1} or 520 cm^{-1} appears in Figs. 6A and 6B of this application, it is inherent that the silicon oxide film has no dopant of boron or phosphorous. Such inherency further establishes the specification support for the claimed lack of dopants now specified to be boron or phosphorous. See MPEP §2163.07(a) citing In re Reynolds, 170 USPQ 94 (CCPA 1971) and In re Smythe, 178 USPQ 279 (CCPA 1973).

Page 15, lines 11-14 of the outstanding Action would essentially ignore the fact that Figs. 6A and 6B of this application have no showings of peaks at 670 cm^{-1} or 520 cm^{-1} and the further fact that this lack of a showing of such peaks proves the absence of boron or phosphorous. See item 6 of the attached Declaration of Professor Kimura setting forth that the absence of any showing of such peaks at 670 cm^{-1} or 520 cm^{-1} makes the absence of dopants of boron and/or phosphorus clear. Thus, the argument of page 15, lines 11-16 of the

outstanding Action that the showings of Figs. 6A and 6B are closer to the Raman spectra for doped silica than for pure silica are clearly without merit.

The analysis at page 15, lines 14-16 of the outstanding Action is further faulty in noting that "[i]n Fig. 1 [of the **Journal of Non-Crystalline Solids** article], a pure fused silica should have a spike at 485 and a peak at 440 cm^{-1}, while Figs. 6A-B only show a peak at ~ 490 without a spike. As noted in item 7 of the attached Declaration of Professor Kimura, "the person of ordinary skill in the art would realize that the arbitrary units for intensity in these two different Figures are just that and that the scale for wavelength is also not intended to be highly precise. They would further note that the leading spike of the series of spikes ranging between about 440 to just under 500 cm^{-1} are in the correct area to correspond with the leading spike and trailing peak noted in the outstanding Action."

Accordingly, the rejection of Claims 9-11, 14, 15, 25-46, and 48-53 under the first paragraph of 35 U.S.C. § 112 is traversed for all the above noted reasons

Turning to the rejection of Claims 9-11, 14, 15, 24-29, 34-45, and 48-53 under 35 U.S.C. § 103(a) as being unpatentable over Rogers in view of Lee, it is noted that page 4 of the outstanding Action presents an analysis of independent Claim 9 subject matter that is clearly improper in failing to consider limitations recited therein that the PTO has objected to as being drawn to new matter and asserted to be the basis for the rejection of all the pending claims under the first paragraph of 35 U.S.C. §112. Similarly, the outstanding Action presents an analysis of independent Claims 25-29 and 36 that is clearly improper in failing to again consider these same claim limitations. This approach to ignoring express claim limitations violates both the MPEP and case law guidelines.

With regard to MPEP guidelines, MPEP 706.03(o)(3) notes that that "[a]s to any other appropriate prior art or 35 U.S.C. 112 rejection, the new matter must be considered as part of

the claimed subject matter and cannot be ignored." MPEP §2143.03further notes that the case of Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem 738 F.2d 453 (Fed. Cir. 1984) sets forth that even if the negative limitations do not appear in the specification as filed, it is error to disregard these limitations when determining whether the claimed invention would have been obvious in view of the prior art. In addition, MPEP §706.02(j) requires that the prior art reference (or references when combined) must teach or suggest all the claim limitations to establish a *prima facie* case of obviousness and that MPEP §2143.03 also states that to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

As the outstanding Action has clearly improperly ignored the limitations of the claims it asserts are "new matters," no *prima facie* case has been established and the rejections offered as to Claims 9-11, 14, 15, 24-46, and 48-53 should all be withdrawn.

Besides improperly ignoring the limitations characterized in the outstanding Action as "new matters," page 4 of the outstanding Action further errs by alleging that the teachings of Rogers somehow suggest that the "dislocation density" in the vicinity of the grooves is "minimized." This is apparently based on the misstatement that Rogers melting and/or remelting are somehow "annealing" or that simply raising a pure oxide and an oxide doped with boron and phosphorous to the same temperature inherently results in the same dislocation density of independent Claims 9, 25, 28, and 29 or the claimed ring structures of independent Claims 26, 27, and 36. However, in order to establish inherency, MPEP §2112(IV) requires more than an assertion; instead, the PTO requires the examiner to

"provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art." This requirement has not been met here.

In addition, the comments presented as to Documents 2-4, 6-9, 12-17, 19-22, and 24 render the assumption in the outstanding Action that the temperature alone will determine the changes undergone by the materials to which it is applied as being clearly without merit.

Accordingly, the theory that Rogers inherently teaches the subject matter of the claimed dislocation density and ring structures or teaches something inherently resulting in this claimed subject matter is also without merit.

Accordingly, the PTO must explain how the Rogers use of doped silicon oxide that has a melting temperature lowering dopant of boron or phosphorous to perform reflow for planarization can be said to teach the subject matter of the above-noted independent claims prohibiting the presence of such doped silicon oxide that has a melting temperature lowering dopant of boron or phosphorous. In addition, the PTO must explain how the Rogers use of doped silicon oxide that has a melting temperature lowering dopant of boron or phosphorous to perform reflow for planarization can be said to be somehow disclosed to be part of an "annealing ... so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized." Note col. 5, lines 55-62 of Rogers disclosing that the silicon dioxide layer 19 is to be formed to a thickness of 2.5 microns with 3-9 weight % impurities such as phosphorus or boron, for example. This need for dopants in the silicon oxide could not be clearer. nor could the need for the SiN layer to block diffusion of the dopant into the underlying structure be any less clear. See col. 3, lines 35-37 and lines 49-52.

Clearly, Rogers includes no disclosure or suggestion of the claimed absence of a reflow-method using doped silicon oxide for planarization, the doped silicon oxide containing

a melting-temperature-lowering dopant **of boron or phosphorus** for lowering the melting-temperature of the silicon oxide. Note further that col. 6, lines 18-22, of Rogers state that the doped glass is melted and reflowed by applying a temperature of about 950 degree to 1,150 degree C. Further, col. 6, lines 26-29, of Rogers state that the process collapses the voids 21-21 and reflows the upper surface 26 of the glass to a substantially level topography, the main objective of Rogers.

Further, Rogers fails to teach or suggest the claimed step of depositing oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant of boron and phosphorous. Col. 5, lines 55-62, of Rogers state that the doped silicon dioxide glass layer 19 is formed to a thickness of about 2.5 microns containing 3-9 weight percent of impurities such as phosphorus or boron, e.g., using the low pressure chemical vapor deposition technique.

Furthermore, Rogers is silent about changing the ring structure of the oxide films by annealing the semiconductor substrate without melting the oxide films. As indicated above, col. 6, lines 18-22, of Rogers state that the doped glass is melted and reflowed.

Turning now to Lee, there is no disclosure or suggestion of the claimed method that is done without using any melting-temperature-lowering dopant **of boron or phosphorus** for lowering the melting-temperature of the silicon oxide. Col. 4, lines 51-57, of Lee state that the layer 23 is formed from precursors, together with dopants, provided the doping level in the layer 23 is lower than in the layer 25 so that the layer 25 will have a lower flow temperature than layer 23. Moreover, col. 4 , lines 58-60, of Lee state that the flow properties of dielectrics deposited from BPTEOS are substantially influenced by the percentages of included boron and phosphorous. Further, claims 1 and 13 of Lee prescribe the

step of depositing a filler material upon said thermal stress relief layer, said filler material having a flow temperature which is lower than the flow temperature of said thermal stress relief layer, claims 5 and 6 of Lee sate that the filler material contains dopant of boron and phosphorous. Furthermore, claim 13 of Lee prescribes the step of heating the flowable filler material to cause the filler material to flow.

Further, Lee fails to teach or suggest the claimed depositing of oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant of boron and phosphorous. Col. 4, lines 31-38, of Lee teaches the decomposition of TEOS in the presence of phosphorous and boron dopants in a reactor.

Furthermore, Lee is silent about changing a nring structure of the oxide films by annealing the semiconductor substrate so as not melt the oxide films. Col. 5, lines 7-16, of Lee state that after filler material 25 has been deposited, it is flowed by heating it, either in a furnace or by a rapid thermal anneal (RTA) process.

Clearly, the proposed combination of Rogers and Lee does not cure the deficiencies of Rogers, because both references fail to teach or suggest claimed method, which does not use the reflow-method with the doped silicon oxide for planarization.

Moreover, the outstanding Action fails to present a reasonable motivation as to why the artisan would have abandoned the main objective of Rogers In terms of the col. 6, lines 26-29, described intent to collapse the voids 21-21 and to reflow the upper surface 26 of the glass to a substantially level topography that requires the presence of boron or phosphorous by abandoning the use of boron and phosphrus. Any proposed modification that would render a reference unsatisfactory for its intended purpose is generally held not to be an obvious one. See In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Accordingly, the rejection of independent Claims 9, 25-29 and 36 as being unpatentable over Rogers in view of Lee is traversed for all the above noted reasons.

As Claims 10, 11, 14, 15, 34, 35, 37-45, and 48-53 depend from one of the above noted independent claims, they are each believed to define patentably over the applied references for the same reason their respective base independent claim does. In addition, each of these dependent Claims adds subject matter not taught or suggested by these relied upon references. Note, for example, the width recited by Claim 51 is not taught or suggested by either Rogers or Lee and that the ability to obtain such a fine width is a clear advantage. The assertion that criticality has not been established at page 12 of the outstanding Action is without merit.

The rejection of Claims 30-33 and 46 is further traversed as the teachings of Dash do not cure the deficiencies in Rogers or Lee that were noted above. In addition, the need for the SiN layer to block diffusion of the dopant into the underlying structure of Rogers is clear. See col. 3, lines 35-37 and lines 49-52. Thus the apparent suggestion that the artisan would be motivated to eliminate this SiN barrier layer needed to block diffusion of the dopant into the underlying structure of Rogers is without merit. Likewise without merit is the attempt at page 13 of the outstanding Action to somehow equate the requirement of Claims 30-33 for direct deposit of the oxide films on the walls of the groove to be "a dimension or ... another variable" requiring a showing of criticality.

As no further issues are believed to remain outstanding in this application, it is believed that this application is clearly in a condition for formal allowance and an early and favorable action to this effect is, therefore, respectfully requested.

Respectfully submitted,

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most common methods. Viscosity between 10^6–1 Pa·s (10^7–10 P) is measured with a Margules viscometer, a calibrated instrument which measures the force exerted by molten glass upon a rotating spindle. The softening point of a glass cannot be defined by a precise viscosity. However, ASTM C338 defines the softening point as the temperature at which a uniform fiber of glass 0.55–0.75 mm diameter and 23.5 cm long elongates under its own weight at 1 mm/min when the upper 10 cm is heated at 5°C/min. For glass having a density of 2.50 g/cm^3, this corresponds to a viscosity of $10^{6.6}$ Pa·s ($10^{7.6}$ P). The exact viscosity is a function of density and surface tension. The annealing point is the temperature that corresponds to a viscosity of approximately 10^{12} Pa·s (10^{13} P) (ASTM C336 and C598). At the annealing point, internal stress is reduced to an acceptable value in about 15 min. The strain-point temperature is the lower end of the annealing range and is approximately $10^{13.5}$ Pa·s ($10^{14.5}$ P) (ASTM C336 and C598). Internal stresses are reduced to an acceptable level in approximately four hours at the strain-point temperature.

Glass is usually melted and fined at viscosities between 5 and 50 Pa·s (50–500 P) but forming and final viscosity requirements vary greatly. The ranges of viscosity for various forming methods are compared in Figure 7.

Viscosities of glass are compared qualitatively. A hard glass has a high softening point and a soft glass has a lower softening point. Long and short refers to the temperature difference between the softening and strain point of glass. A long glass has a large temperature difference between its softening and strain point, ie, it solidifies (sets up) slower than a short glass as temperature decreases.

Thermal. *Expansion.* The thermal expansion of a glass determines the range of materials to which it can be safely sealed. It also affects the ability of the glass to survive thermal shock or cycling. The usefulness of glass as a heat exchanger or a thermal barrier, and its ease of melting and forming, depend on its heat-transfer properties and emissivity. The upper use temperature is a function of all of these properties.

Like most materials, glass expands when it is heated and contracts when it is cooled. If the thermal cycling is slow enough, there is virtually no hysteresis effect. Linear expansion, $\Delta L/L$, is the change in length per initial length. Generally, the expansion is proportional to temperature up to 300°C or more, depending on the glass. The slope of the linear expansion vs temperature curve, the linear thermal expansion coefficient, α, is therefore virtually constant between 0 and 300°C for most glasses, and thus α_{0-300} is a useful property for comparisons (see Table 4). As the temperature of the glass rises to near the set point (strain point + 5°C), the thermal expansion increases more rapidly (compare Figure 1, which is a volume–temperature curve for a general glass). The volume–temperature curve is analogous to linear expansion (length–temperature) curves. The density, ρ, which depends on the temperature, is easily calculated from the density at room temperature and the appropriate linear thermal expansion coefficient.

The sealing of glasses to either metals or other glasses depends on the thermal expansion mismatch of the two materials as well as their rheological and elastic properties (59). The materials must be heated to a point where the softer glass flows and intimately contacts the other material. In the case of glass-to-glass seals, the glasses flow together and bond extremely well. For glass-to-metal seals, however, a complicated and rigorously controlled oxidation-reduction re-

Properties

Rheological. The viscosity of a glass determines its melting, forming, and annealing procedures as well as the limitations of its use at high temperature. Viscosity is ordinarily measured between 10^{13} and 10 Pa·s (10^{14} and 100 P); at room temperature it is greater than 10^{19} Pa·s (10^{20} P). The rapid but smooth change of viscosity with temperature is shown for several glasses in Figure 6. Compositions and properties are shown in Tables 3, 4, and 5. The effect of modifiers on the viscosity of glass at high temperature depends on their polarizability or ionic field strength (58). Low field-strength modifiers decrease the viscosity of silica more than high field-strength ones. At low temperature, the effects of a modifier on viscosity are largely controlled by its coordination number. Modifiers with higher coordination numbers tend to increase low temperature viscosity as a result of packing restraints (see RHEOLOGICAL MEASUREMENTS).

Reference points on the viscosity–temperature curve in Figure 7 have been chosen to characterize properties of an individual glass and to facilitate comparisons of similar glasses. Those used most frequently are the working, softening annealing, and strain points. Definitions of these selected points are given by ASTM. The working point of a glass is the temperature at which its viscosity is exactly 1 kPa·s (10^4 P). At this viscosity, glass is sufficiently fluid for forming by

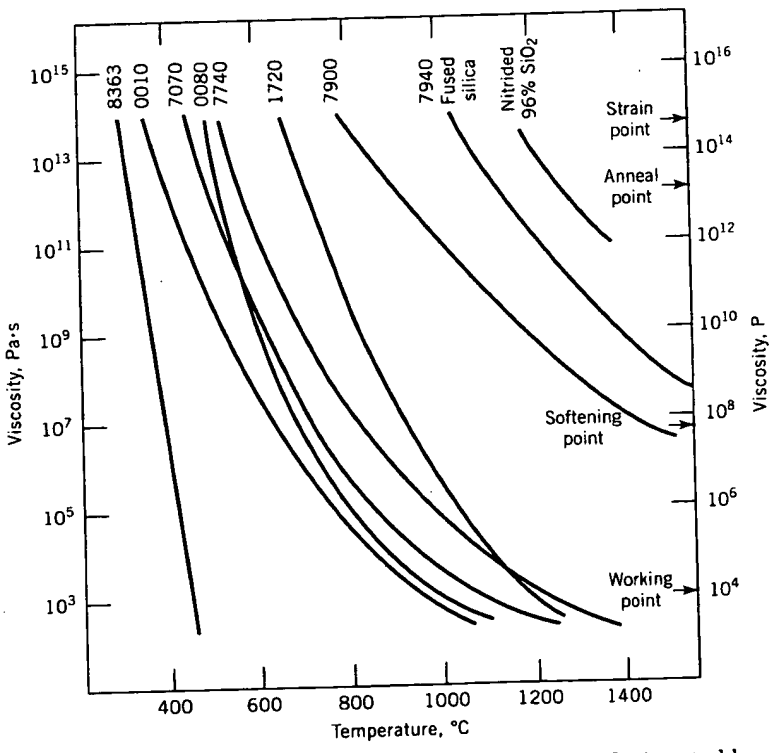

Fig. 6. Viscosity vs temperature for some commercial glasses designated by glass cod (see Table 3). Courtesy of Corning Inc.

LISTING AND COMMENT ON DOCUMENTARY EVIDENCE

[1] S. A. Campbell, "The Science and Engineering of Microelectronic Fabrication," Oxford University Press (1966), p. 324;

Lines 9-10 of this textbook state that the toxicity of phosphine and silane used in PSG deposition, and lines 16-18 state that the need for hazards chemicals such as phosphine is eliminated in TEOS deposition. Therefore, it is clear that the term "TEOS" means "non-doped TEOS," which eliminates the usage of impurity atoms such as boron (B) and phosphorus (P) atoms in the deposition.

On the contrary, Lee et al. employ the terms "BPTEOS" and "PTEOS" to as to specify the incorporation of impurity atoms. For example, in BPTEOS, 3 percent boron and 3 percent phosphorous by weight is added (See column 4, lines 28-38). In column 4, lines 28-38, Lee et al. clearly define that "the expression 'depositing a layer of BPTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence of phosphorous and boron dopants in a reactor."

Furthermore, in column 4, line 65 to column 5, line 3, Lee et al. clearly define that "the expression 'PTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence of phosphorous with no significant amount of boron dopants in a reactor."

[2} A. Hamada et al., "A new aspect of mechanical stress effects in scaled MOS Devices," IEEE Transaction on Electron devices, Vol. 38, No. 4, April, 1991, pp895-900;

In Table 1, set of material values of Young's module E(GPa), Poisson's ratio ν and thermal expansion coefficient α (10^{-6}/°C) used in mechanical stress simulation for Si, SiO_2, PSG, and Al are shown. Table 1 shows different materials have different material values, which give different mechanical stresses. That is, if materials are different, the defects generated by mechanical stresses vary depending on material values.

As A. Hamada et al. disclose, the dislocation density is not determined only by process temperatures, but it depends on material values of Young's modulUS E(GPa), Poisson's ratio ν and thermal expansion coefficient α (10^{-6}/°C), it is clear that the assertion that the claimed dislocation inherently occurs in the heating step of the prior art even if boron and phosphorous dopants are contained in the silicon oxide film is not based on a sound scientific basis.

Furthermore, please note that the term "SiO_2" is clearly differentiated from the term "PSG" in A. Hamada et al., because the nomenclature of "SiO_2" is accepted by the artisan as a non-doped material, which excludes the incorporation of impurity atoms such as boron (B) and phosphorus (P) atoms. To the contrary, Rogers employ the terms "doped silicon dioxide glass layer 19" (See, for example, column 5, lines 55-59) and "doped glass" (See, for example, column 6, lines 18-22) so as to specify the incorporation of impurity atoms. The expression "BPSG" is generally understood by those skilled in the art to mean SiO_2 layer containing phosphorous and boron dopants, the expression "BSG" is generally understood by those skilled in the art to mean SiO_2 layer containing boron dopants, and the expression

"PSG" is generally understood by those skilled in the art to mean SiO_2 layer containing phosphorous dopants.

[3] K. Ishimaru et al., "Mechanical stress induced MOSFET punch-through and process optimization for deep submicron TEOS-03 filled STI devices" in VLSI Tech. Dig. Tech. Papers, June 1997, pp. 123-124;

As co-authors of this document, co-inventors of the present invention, namely *K. Umezawa* and *N. Tuchiya* are included, because this document is partly based upon the disclosure of the present invention. As stated on page 1223, left column, lines 14-16, mechanical stress induced defect generation accompanying the MOSFET punch-through in TEOS-O_3 filled STI structure is reported for the first time, and Fig. 6 shows a relationship between the defect density and annealing temperature. The relationship shown in Fig. 6, is substantially the same result as the relationship shown in Fig. 4 of the present invention. That is, we believe there was no research work, which measured defect density associated with STI filled with TEOS oxide film and determined the relationship between the defect densities and annealing temperature in TEOS-O_3 filled STI structure, until the pioneering work of the present inventors.

Therefore, if the PTO asserts that the claimed dislocation inherently occurs in the heating step of the prior art even if boron and phosphorous dopants are contained in the silicon oxide film being melted, the PTO must show a similar relationship to that shown in Fig. 4 of the present invention in the prior art, because the initial burden is on the PTO to show the claimed dislocation inherently occurs in the heating step of the prior art.

[4] H.S. Lee et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," in 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 158-159;

Size dependency of defects is disclosed on page 158, left column, line 2 from the bottom to right column line 7. Once again, defects depend on more than temperature. Page 19, lines 10-14 and page 27, line 34 to page 28, line 4 of the specification show a width of 0.3 μm. Figs. 5 and 9 disclose L/S=0.35 μm/0.35 μm, which means the width of the groove is 0.35 μm. Page 6, line 6 to page 7, line 8, page 29, lines 25-35, and Fig. 11 of the application show the defect density is reduced at an aspect ratio of less than 10. As page 19, lines 10-14 state depth of 1 μm, the grooves can have a width of 0.1 μm to keep the aspect ratio of less than 10. Furthermore, Eq. (3) shown on page 7 prescribe the relation:

$$l_1/l_2 \leq 1.5 \qquad \ldots (3)$$

where l_1 is the width of groove and l_2 is the width of the device region (SDG region) sandwiched by the grooves. Since, for example, page 11, lines 10-16 state the width of the device region is 0.3 μm, the width of groove must be less than or equal to 0.2 μm to satisfy the Eq. (3).

Rogers fail to show a groove having such a width. Essentially, since the stress relief oxide layer 16 must have the thickness of about 30 to 100 nm, the polycrystalline silicon etch-stop layer 17 must have the thickness of about 100 to 300 nm, and the silicon nitride

barrier layer 18 must have the thickness of 100 to 250 nm to appropriately provide the functions of the respective layers, such as blocking the diffusion of dopant from the doped silicon dioxide glass layer 19, the width of groove must be greater than 0.5 μm.

Similarly, Lee discloses trenches as narrow as 0.6 μm and as wide as 30 μm, but fail to show a trench narrower than 0.5 μm (see column 3, lines 39-3)

Although the size limitation is only directly incorporated into Claim 51, the Examiner should consider the size dependency of defects, and the Examiner must show claimed dislocation density generated in the corresponding device region in a vicinity of the grooves, which is less than $1\mu m^{-2}$, because the initial burden is on the Examiner to show the claimed dislocation density as inherent is more fully noted in the remarks.

[5] K. Shiozawa et al., "Electrical Characteristics of Ultra-fine Trench Isolation Fabricated by a New Two-Step Filling Process," Jpn., J. Appl. Physics, Vol. 35 (1996), pp. L1625-L1627;

Employment of soft TEOS-SiO_2 and hard high-density SiO_2 in two-step oxide filling is disclosed on page L1625, left column, lines 20-21. The term "soft" and "hard" mean that, if materials are different, the defects generated by mechanical stresses ascribable to the filling materials in the trench vary depending on hardness of the filling materials.

[6] G. Scott et al., "NMOS drive current reduction caused by transistor and trench isolation induced stress," in IEDM Tech Dig., 1999, pp. 827-830;

The results of SUPREM simulation are illustrated in Fig. 8, which show that stress in the diffusion area varies with the size of the diffusion, increasing from 2.4 to 5.7 X $10^9 dyne/cm^2$ as gate length L shrinks from 2.4 to 1.2 μm (See page 829, right column, lines 5-2 from the bottom).

Thus, it is evident that the dislocation density generated in the corresponding device region in a vicinity of the grooves varies strongly with the size of the subject devices.

[7] P. Ferreira et al., "Elimination of stress induced silicon defects in very high-density STRAM structures," in Proc. ESSDERC, 2001, pp227-230;

Silicon defects induced by mechanical stress is reported. As Fig. 5 shows impact of gate material intrinsic stress and oxidation induced stress, the stress varies with gate materials (See page 227, left column, line 4 to right column lines 5-2 from the bottom). The fact disclosed in P. Ferreira et al. implies that the defects generated in the corresponding device region in a vicinity of the grooves vary with material values of the filling materials in the grooves.

[8] R.A. Bianchi et al., "Accurate Modeling of Trench Isolation Mechanical Stress Effect on MOSFET Electrical Performance," in IEDM Tech Dig., 2001, pp.117-120;

of phosphorous and boron dopants in a reactor." Furthermore, in column 4, line 65 to column 5, line 3, Lee et al. clearly define that the "expression 'PTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence of phosphorous with no significant amount of boron dopants in a reactor."

[19] K Okonogi et al., "Defect control of STI process technology," A., NEC Res. Dev. (Japan), vol. 42, no. 1, pp.59-63, (2001);

K. Okonogi et al. teach that even in 2001, five years layer than application date of the present invention, "although it is believed that dislocation is caused by localized stress near trench, there have been no systematically studies on the relationships between the localized stress and dislocation density for various STI process (See page 59, left column, lines 19-23).

Furthermore, K.Okonogi et al. once again teach that different trench structure have different types of mechanical stress (See page 59, right column, lines 22-24).

[20] I.V. Peidous et al., "Critical states of stress evolution in silicon structures of ULSI with shallow trench isolation," ULSI Process Integration, Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol. 99-18), pp.243-254 (1999);

I.V. Peidous et al. teach that even in 1999, three years later than application date of the present invention, "the analysis of stress in semiconductor structure is a complex task..... As soon as the stress state of a structure is determined, however another question rises – what reasonable criteria should be used for linking the stress and device structure vulnerability to defects (See page 248, lines 10-19)."

I.V. Peidous et al. cite the documentary evidence [3] (K. Ishimaru et al.,) as a pioneering work, which compared defect densities in STI device element (See page 244, lines 1-5). Thus, it can be concluded that there was no research work determining the relationship between the defect densities and annealing temperature in TEOS-O_3 filled STI structure known to these authors until the pioneering work of the present inventors.

I.V. Peidous et al. further teach "characteristics of an STI physical structure which control stresses and, therefore, stress-induced defect formation include geometric parameters and mechanical properties of the materials integrated in STI" (See page 249, lines 24-26), not just the temperature being applied.

Furthermore, in Fig. 6, intrinsic stresses in LPCVD TEOS film, as-deposited and densified, are shown. And I.V. Peidous et al. disclose that, by densification of the TEOS film, the mechanical property of the TEOS film is transformed into that of thermal oxide film defects (See page 250, lines 1-11). Because the original meaning of "the thermal oxide" exclude the incorporation of impurity atoms such as boron (B) and phosphorus (P) atoms, the teaching of I.V. Peidous et al. confirms that the term "TEOS" means "non doped TEOS," which excludes the impurity atoms. On the contrary, Lee et al. employ the terms "BPTEOS" and "PTEOS" so as to specify the incorporation of impurity atoms.

Relationships between mechanical stress induced by shallow trench isolation and geometry variations, such as Active Area (AA) size & shape, gate location inside AA are reported. The fact disclosed in R.A. Bianchi et al. implies that the defects generated in the corresponding device region in a vicinity of the grooves depend on the geometry variations.

[9] W.G. En et al., "Reduction of STI/active Stress on 0.18m SOI Devices Through Modification of STI process," in IEEE Int. SOI Conf., 2001, pp85-86;

The effect of STI stress on the device characteristics is measured by using test transistors with different active sizes. The facts disclosed in W.G. En et al. implies that the defects generated in the corresponding device region in a vicinity of the grooves depend on the geometry variations.

[10] J.W. Sleight et al., "Stress Induced Defects and Transistor Leakage for Shallow Trench Isolated SOI," IEEE Electron Device Letters, Vol. 20, No. 5, May 1999 pp. 248-250;

In J.W. Sleight et al., the documentary evidence [3] (K. Ishimaru et al.,) is cited as a pioneering work (See page 248, left column, lines 23-26). No other research work determining the relationship between the defect densities and annealing temperature in TEOS-O_3 filled STI structure until the pioneering work of the present inventors was known to Sleight et al.

[11] D.Ha et al., "Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices," IEEE Transaction on Electron devices, Vol. 46, No. 5, May 1999, pp940-946;

In D. Ha et al., the documentary evidence [3] (K. Ishimaru et al.,) is cited as a pioneering work (See page 940, right column, lines 4-8). Once again, there was no research work determining the relationship between the defect densities and annealing temperature in TEOS-O_3 filled STI structure until the pioneering work of the present inventors again was known to these authors.

[12] C. Gallon et al., "Electrical Analysis of Mechanical Stress Induced by STI in short MOSFETs Using Externally Applied Stress," IEEE Transaction on Electron devices, Vol 51, No. 8, August 2004, pp. 1254-1261;

C. Gallon et al. teach that even in 2004, eight years later than application date of the present invention, "stress is difficult to measure locally and is also difficult to simulate, since there is a critical lack of data for many thin-film material used in technological process (See page 1254, right column, lines 11-15)".

As stated on page 1254, left column, lines 23-27, the stress depends on mechanical properties and thermal coefficient mismatches, the dislocation densities generated in the corresponding device regions in vicinities of the grooves vary for different materials filled in the grooves.

[13] P.Ferreira et al., "Finite Element Optimization of a MOSFET Structure: The Role of Interlayer material for Residual Stress Reduction," in IEDM Tech Dig., 2005, pp. 503-506;

As shown in Fig. 12, the term "TEOS" is clearly distinguished from the term "BPSG" in P.Ferreira et al., because, to a person having ordinary skill in the art, the nomenclature of "TEOS" is accepted as a non-doped material, which excludes the incorporation of impurity atoms such a boron (B) and phosphorus (P) atoms. On the contrary, Lee et al. employ the terms "BPTEOS" and "PTEOS" so as to specify the incorporation of impurity atoms. For example, in BPTEOS, 3 percent boron and 3 percent phosphorous by weight is added (See column 4, lines 28-38). In column 4, lines 28-38, Lee et al. clearly define such that "the expression 'depositing a layer of BPTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence of phosphorous and boron dopants in a reactor." Furthermore, in column 4, line 65 to column 5, line 3, Lee et al. clearly define such that the "expression 'PTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence of phosphorous with no significant amount of boron dopants in a reactor."

P. Ferreira et al. teach that the device containing BPSG have been found free from dislocations, whereas the device that did not contain BPSG exhibit dislocation loops (See page 504, right column, lines 2-9)." Thus, the PTO cannot show the claimed dislocation density generated in the corresponding device region in a vicinity of the grooves is just because of heat because materials filled in the groove are different. The teaching of P.Ferreira et al. clearly negates the outstanding Action assertion that the claimed dislocation inherently occurs in the heating step of the prior art even if boron and phosphorous dopants are contained in the silicon oxide film being melted.

[14] C. Gallon et al., "Electrical analysis of mechanical stress induced by shallow trench isolation," ESSDERC 2003, Proceedings of the 33rd European Solid-State Device Research Conference, 16-18 September 2003, pp.359-362;

C. Gallon et al. teach that even in 2003, seven years later than application date of the present invention, "stress is difficult to measure locally and is also difficult to simulate, since there is a critical lack of data for many thin-film material used in technological process (See page 359, right column, lines 9-6 from the bottom)."

From Eqs. (1) and (2), which show that the stress depends on geometrical dimensions and mechanical properties such as the Young's Modulus E, it can be understood that the dislocation densities generated in the corresponding device regions in vicinities of the grooves vary for different materials filled in the grooves and different geometries and is not simply a matter of the temperature applied.

[15] S.H. Shin et al., "Data retention time and electrical characteristics of cell transistor according to STI materials in 90 nm DRAM," J. Korean Phys. Soc. (South Korea), vol. 43, no. 5, November 2003, pp.887-897;

Fig. 9 shows the shear stress characteristics of the structure in which only HDP oxide is filled in the STI groove is different from the structure in which HDP oxide and poly-

silazane (P)-SOG oxide are filled in the STI groove. Thus, S.H. Shin et al. teach that the dislocation densities generated in the corresponding device regions in vicinities of the STI grooves vary for different materials filled in the STI grooves. Once again, temperature alone does not determine dislocation density.

[16] A. Armigliato et al., "Strain analysis in sub-micron silicon devices by TEM/CBED, IOP Publishing, "Microscopy of Semiconducting Materials 2001," Proceedings of the Royal Microscopical Society Conference, Oxford University 25-29 March 2001, pp.467-472;

Fig. 3 shows differences of the tensor traces for a sample in which a lower HDP oxide is covered by an upper TEOS oxide as shown in Fig. 1 (a) and another sample in which the lower HDP oxide is covered an upper HDP oxide as shown in Fig. 1 (b). Thus, A. Armigliato et al. also teach that the dislocation densities generated in the corresponding device regions in vicinities of the STI grooves vary for different materials filled in the STI grooves.

Please note on page 468, lines 12-14, which state that the oxides are annealed at a very high temperature to obtain near thermal oxide characteristics. Because the original meaning of "the thermal oxide" exclude the incorporation of impurity atoms such as boron (B) and phosphorus (P) atoms, the teaching of A. Armigliato et al. confirms that the term "TEOS" means "non doped TEOS," which excludes the impurity atoms.

[17] Jin-Hwa Heo et al., "Void free and low stress shallow trench isolation technology using P-SOG for sub 0.1 μm device," 2002 Symposium on VLSI Technology Digest of Technical Papers, June 11-13, 2002, pp.132-133;

Fig. 5 shows P-SOG has lower compressive stress than HDP oxide because of its lower density (See page 132, right column, lines 3-4). Thus Jin Hwa Heo also teach that the dislocation densities generated in the corresponding device regions in vicinities of the STI grooves vary for different materials filled in the STI grooves.

As illustrated by FT-IR spectra shown in Fig. 3, the nomenclature of "SiO_2" is used to indicate a non doped material, which excludes the incorporation of impurity atoms such as boron (B) and phosphorous (P) atoms as a person having ordinary skill in the art would understand.

[18] T. Nakamura, "Novel pulse pressure CVD for void free STI trench TEOS fill," 2001 IEEE International Symposium on Semiconductor Manufacturing, ISSM 2001, Conference Proceedings, October 8-10, 2001, pp.117-120;

As shown in Table 2, the TEOS CVD process condition uses only TEOS gas as a source gas, and the employment of dopant gas containing such as boron (B) atoms and/or phosphorous (P) atoms is eliminated in LP-CVD equipment. On the contrary, Lee et al. employ the terms "BPTEOS" and "PTEOS" so as to specify the incorporation of impurity atoms. For example, in BPTEOS, 3 percent boron and 3 percent phosphorous by weight is added (See column 4, lines 28-38). In column 4, lines 28-38, Lee et al. clearly define that "the expression 'depositing a layer of BPTEOS' is generally understood by those skilled in the art to mean the deposition of a dielectric layer by decomposition of TEOS in the presence

[21] K.F. Dombrowski et al., "Investigation of stress in STI using UV-Raman spectroscopy," ESSDERC '99, Proceedings of the 29th European Solid-State Device Research Conference, 13-15 September 1999, pp.196-199;

Figs. 3-5 shows mechanical stresses for the groups having a width and spacing of 3.0, 2.0, 1.0, 0.9, 0.8, 0.7, 0.6, 0.5, 0.45, 0.4 and 0.35 μm from the right, and teach that the trench dimension has a large impact on the stress level. The dependence of the stress on the trench dimension is complicated, because as the lines become narrower, the stress increases up to the 1.0 μm group, and then the stress decreases again form the 1.0 μm group (See page 198, right column, lines 7-18)." Once again, temperature alone will not dictate the stress.

[22] Soon Moon Jung et al., "High density low power full CMOS SRAM cell technology with STI and CVD Ti/TiN barrier metal," ICVC '99. 6th International Conference on VLSI and CAD, October 26-27, 1999, pp.119-121;

Soon Moon Jung et al. teach that the magnitude of the stress depends on not only the IC process but also on active pattern shapes (See page 119, left column, lines 28-29). The teaching of Soon Moon Jung et al. clearly negates the theory that temperature alone controls.

[23] Daewon Ha et al., "Anomalous junction leakage current induced by STI dislocations and its impact on dynamic random access memory devices," IEEE Trans. Electron Devices, vol. 46, no. 5, pp.940-946 (1999);

Daewon Ha et al. cite the documentary evidence [3] (K. Ishimaru et al.,) pioneering work (See page 940, right column, lines 4-8). Thus, it can be concluded there was no research work determining the relationship between the defect densities and annealing temperature in TEOS-O_3 filled STI structure, known to these authors until this pioneering work.

[24] G. Simpson et al., "Sub-0.18 μm STI by APCVD TEOS: Ozone," European Semiconductor, vol. 21, no. 9, pp.31-34 (1999).

Fig. 6 (page 33, the third Figure from the top) shows that the film stress depends on deposition temperature of TEOS, and higher-temperature exhibit higher compressive stress post-dense (See page 34, left column, lines 6-9). However, deposition temperature of doped glass stated in Rogers et al. is about 500-800°C (See column 5, lines 59-62), which is higher than normally employed deposition temperature of TEOS.

Then in view of the teaching of G. Simpson et al., it clearly cannot be shown that the claimed dislocation density generated in the corresponding device region in a vicinity of the grooves is inherent in Rogers.

Fig. 1 (Page 31, the top Figure in the central column) shows a schematic view of a monoblok of TEOS: Ozone liner injector, by which reactant (TEOS) and oxidizers (O_2/Ozone) are injected in separate laminar curtains without employing dopant gas (See page 31, right column, lines 7-10). Therefore, it is clear that the term "TEOS" means "non doped

TEOS," which eliminates the usage of impurity atoms such as boron (B) and phosphorus (P) atoms in the deposition. On the contrary, Lee et al. employ the terms "BPTEOS" and "PTEOS" so as to specify the incorporation of impurity atoms.

List of Documentary Evidences

[1] S. A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, (1996), p.324;

[2] A. Hamada et al, "A new aspect of mechanical stress effects in scaled MOS Devices", IEEE Transaction on Electron devices, Vol. 38, No,4, April, 1991, pp895-900;

[3] K. Ishimaru et al., "Mechanical stress induced MOSFET punch-through and process optimization for deep submicron TEOS-O3 filled STI devices" in VLSI Tech. Dig. Tech. Papers, June 1997, pp.123-124;

[4] H. S. Lee, et al, "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)", in 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 158-159 ;

[5] K. Shiozawa et al, "Electrical Characteristics of Ultra-fine Trench Isolation Fabricated by a New Two-Step Filling Process", Jpn., J. Appl. Physics, Vol. 35 (1996), pp. L1625-L1627 ;

[6] G.Scott, et al, "NMOS drive current reduction caused by transistor and trench isolation induced stress", in IEDM Tech Dig.,1999, pp. 827-830 ;

[7] P. Ferreira, et al, "Elimination of stress induced silicon defects in very high-density sram structures", in Proc. ESSDERC, 2001, p427;

[8] R.A.Bianchi et al, "Accute modeling of trench isolation mechanical stress effect on MOSFET electrical performance," in IEDM Tech Dig., 2001,p.117;

[9] W.G. En et al, "Reduction of STI/active stress on 0.18m SOI devices through modification of STI process," in IEEE Int. SOI Conf.,2001, pp85-86;

[10] J. W. Sleight et. al, "Stress Induced Defects and Transistor Leakage for Shallow

Trench Isolated SOI", IEEE Electron Device Letters, Vol. 20, No,5, May, 1999 pp. 248-250;

[11] D. Ha et. al, "Anomalous Junction Leakage Current Induced by STI Dislocatons and Its Impact on Dynamic Random Access Memory Devices", IEEE Transaction on Electron devices, Vol. 46, No,5, May, 1999 pp940-946;

[12] C. Gallon et al, "Electrical Analysis of Mechanical Stress Induced by STI in short MOSFETs Using Externally Applied Stress", IEEE Transaction on Electron devices, Vol. 51, No,8, pp.1254-1261;

[13] P. Ferreira, et al, "Finite Element Optimization of a MOSFET Structure: The Role of Interlayer material for Residual Stress reduction", in IEDM Tech Dig., 2005, pp.503-506;

[14] C. Gallon et al, "Electrical analysis of mechanical stress induced by shallow trench isolation", ESSDERC 2003, Proceedings of the 33rd European Solid-State Device Research Conference, 16-18 September, 2003;

[15] S.H. Shin et al, "Data retention time and electrical characteristics of cell transistor according to STI materials in 90 nm DRAM", J. Korean Phys. Soc. (South Korea), vol.43, no.5, pp.887-891;

[16] A. Armigliato et al, "Strain analysis in sub-micron silicon devices by TEM/CBED", IOP Publishing, "Microscopy of Semiconducting Materials 2001", Proceedings of the Royal Microscopical Society Conference, Oxford University, 25-29 March 2001;

[17] Jin-Hwa Heo et al, "Void free and low stress shallow trench isolation technology using P-SOG for sub 0.1 μ m device", 2002 Symposium on VLSI Technology. Digest of Technical Papers, June 11-13, 2002, pp132-133;

[18] T. Nakamura, "Novel pulse pressure CVD for void free STI trench TEOS fill", 2001 IEEE International Symposium on Semiconductor Manufacturing, ISSM 2001. Conference Proceedings, October 8-10, 2001, pp117-120;

[19] K. Okonogi et al., "Defect control of STI process technology", A., NEC Res. Dev. (Japan), vol.42, no.1, pp59-63, (2001);

[20] I.V. Peidous et al, "Critical states of stress evolution in silicon structures of ULSI with shallow trench isolation", ULSI Process Integration, Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol.99-18), pp243-254. (1999);

[21] K.F. Dombrowski et. al, "Investigation of stress in STI using UV-Raman spectroscopy", ESSDERC'99, Proceedings of the 29th European Solid-State Device Research Conference, 13-15 September 1999, pp196-199;

[22] Soon Moon Jung et. al, "High density low power full CMOS SRAM cell technology with STI and CVD Ti/TiN barrier metal", ICVC '99. 6th International Conference on VLSI and CAD, October 26-27, 1999, pp119-121;

[23] Daewon Ha et. al., "Anomalous junction leakage current induced by STI dislocations and its impact on dynamic random access memory devices", IEEE Trans. Electron Devices, vol.46, no.5, pp940-946 (1999);

[24] G. Simpson et. al., "Sub-0.18 μ m STI by APCVD TEOS: ozone", European Semiconductor, vol.21, no.9, pp31-34 (1999).

The Science and Engineering of Microelectronic Fabrication

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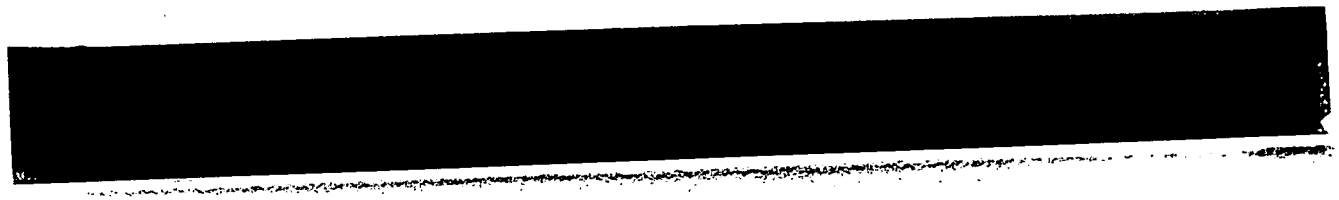
New York *Oxford*
Oxford University Press
1996



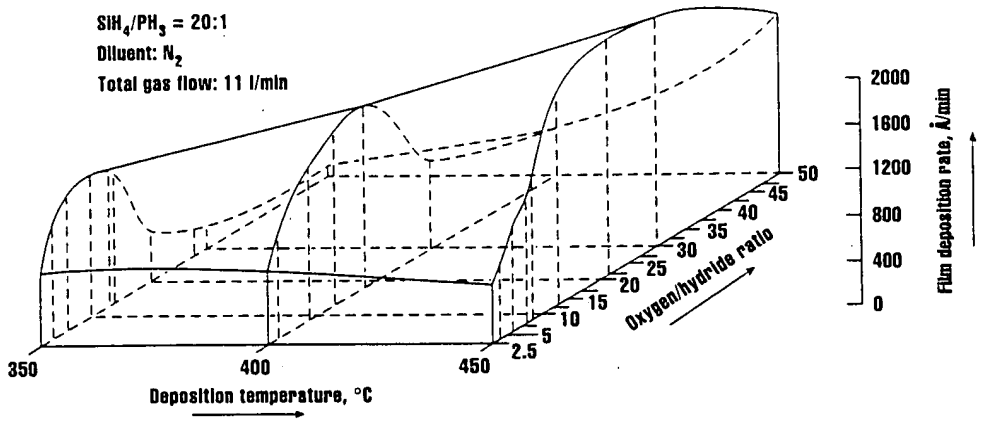


Figure 13-10 Deposition rate of PSG in an APCVD system *(after Kern and Rosler, ®1977, AIP).*

As will be discussed in Chapter 15, it is often desirable to deposit silicon dioxide films with 4 to 12% phosphorus. These phosphosilicate glasses (PSG) soften and reflow at moderate temperatures, smoothing wafer topology and gettering many impurities. PSG can be formed in an atmospheric process by adding phosphine (PH_3). Figure 13.10 shows a typical plot of the deposition rate of PSG versus temperature and oxygen to hydride flow rates. For high oxygen concentration ambients (30:1), the deposition rate increases sharply with temperature and is probably reaction rate limited. For low oxygen containing ambients (2.5:1), the growth rate actually decreases slightly with increasing temperature. The phosphorus content of the film can be controlled by changing the phosphine to silane ratio. Due to the toxicity of phosphine and silane, APCVD systems designed for PSG deposition are generally housed in a vented cabinet. To improve uniformity and step coverage, many PSG and borophosphosilicate glass (BPSG) processes now use organometallic sources such as TEOS (tetraethyloxysilane or $Si(OC_2H_5)_4$). TEOS and ozone can also be used to deposit SiO_2 at about 400°C [10]. TEOS is supplied as a stable, inert, high vapor pressure liquid that is used in a bubbler (see Section 3.8). One of the advantages of using TEOS is the elimination of the need for some of the hazardous chemical handling. The lines from the bubbler must be heated to prevent deposition on the walls of the tubing. Various alternate organometallics have also been investigated. Hexamethyldisiloxane ($(CH_3)_3$-Si-O-Si-$(CH_3)_3$), a linear disiloxane, has also shown excellent characteristics comparable to TEOS [11], but the deposition rate was found to depend on the substrate material. Similar films have also been deposited from hydridospherosiloxanes [12] with wet oxygen at about 500°C.

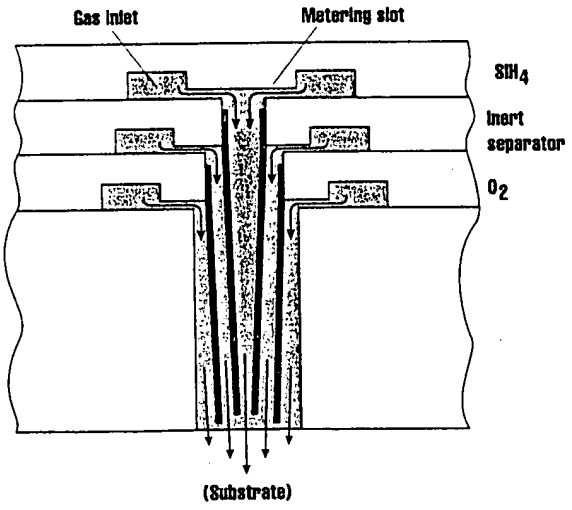


Figure 13-11 Showerhead design used to minimize deposition at the nozzle by maintaining an inert curtain between the reactants.

The major drawback of APCVD is particle formation. While particle formation in the gas phase can be controlled by adding a sufficient amount of N_2 or another inert gas, heterogeneous deposition can also oc-

A New Aspect of Mechanical Stress Effects in Scaled MOS Devices

Akemi Hamada, Takeharu Furusawa, Naoto Saito, and Eiji Takeda, *Senior Member, IEEE*

Abstract—**Deviation in device characteristics due to mechanical stress is investigated experimentally and analytically from the viewpoints of scaling and hot-carrier effects. In scaled MOS devices, the effect of uniaxial stress is reduced. However, the effect of vertical stress, such as mold stress, becomes a serious problem when the vertical stress causes compressive surface stress. Compressive stress has a serious effect on electron trapping in SiO_2. These results provide important guidelines for the manufacture and package design of deep submicrometer devices.**

I. Introduction

As MOS devices are scaled down to the deep-submicrometer region, new reliability problems arise corresponding to each generation. Of these problems, new physical phenomena considered to be related to mechanical stress are more significant for the manufacture and package design of deep-submicrometer devices. This is mainly because several kinds of device degradation resulting from process-induced mechanical stress cause additional reliability problems. This trend calls for a deeper physical understanding and re-examination of ULSI reliability from the viewpoint of mechanical stress.

Zekeriya *et al.* studied the dependence of radiation-induced interface traps on gate-induced strain using gate material as a parameter [1]. Large compressive strain exists at the surface of thick gate electrodes and there are fewer radiation-induced interface traps in thick-gate electrode devices. This suggests that interface trap generation tends to reduce under compressive surface strain. Mitsuhashi *et al.* studied hot-carrier effect on devices with various passivation layers (e.g., PSG, p-SiON, p-SiN, p-SiO) [2]. Under compressive stress, the shift in threshold voltage (ΔV_{th}) is bigger than in nonstressed devices. However, hydrogen effect is also included, so the reason why ΔV_{th} is bigger in compressed devices was not clarified.

This paper investigates the device characteristics by imposing external mechanical stress on a Si chip and experimental results are physically analyzed by mechanical stress simulation (SIMUS 2D/F) [3]. The new findings obtained are as follows: 1) Transconductance deviation $(\Delta G_m/G_{m0})_M$ due to external mechanical stress is reduced, rather than enhanced, in scaled MOS devices because of modulated stress distribution in the channel, and 2) shift in threshold voltage (ΔV_{th}) due to hot-carrier injection increases under external compressive stress because of an increased electron capture rate in SiO_2. These results will provide significant guidelines for the manufacture and package design of deep-submicrometer devices.

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II. Sample Preparation and Measurement Setup

Both n- and p-channel single-drain MOSFET's fabricated on (100) oriented substrates were evaluated. The gate oxide thickness T_{ox} was 10 nm, the gate length L was 0.5–10 μm, and the gate width W was 10 and 100 μm. An external stress ranging from −200 to 200 MPa was applied using the four-point-bending technique, as shown in Fig. 1. The surface stress (σ_x) was calculated from beam analysis using weight (W) precisely controlled by the tensile testing machine (Instron type 1381).

$$M = -Wa \qquad \text{bending momentum}$$

$$a < x < (a + c)$$

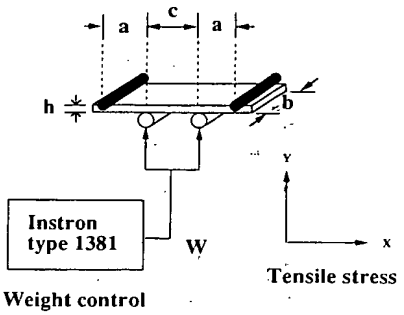
$$Z = bh^2/6 \qquad \text{cross-section coefficient}$$

$$\sigma_x = M/Z$$

$$= 6aW/(bh^2) \qquad \text{surface stress}$$

where a denotes the distance between props, b denotes the chip width, and h denotes the chip thickness. The surface stress σ_x between props is assumed to be uniform. The arrangement used in this study was a) longitudinal, $\sigma_x // (J \perp (011))$ and b) transverse, $\sigma_x \perp (J \perp (011))$, where J indicates the direction of current flow.

A stress analysis program named SIMUS (stress analysis program for multilayer structure) 2D/F, which can analyze the stress state of thin multilayer structures such as LSI devices throughout their manufacturing process, was used. This program has three special features: 1) flexibility to changes in the modeling region in the thin-film deposition process, 2) efficient calculation by reducing the size of the modeling region assuming an equivalent wafer, that is, a thin, stiff, and artificial layer representing the stiffness of the most part of the wafer, and 3) viscoelastic analysis with temperature-dependent material properties. Simulated device structure, which is the same one as the measured samples, is described in Fig. 2. The boundary conditions were: one end in the X direction was fixed along $x = 0$ (Y direction free), another end was movable (symmetry). In the Y direction, the bottom was fixed (X direction free) and the surface was free. The set of material values used is listed in Table I for $T = 0°C$. A dummy region was used to produce an external force with the thermal expansion coefficient of the silicon substrate set to zero. Here, the applied temperature was 0°C, so the viscoelastic effect was ignored.



Schematic Diagram of Measurement Setup;

$\sigma_x = 6W(a/bh^2)$

Fig. 1. Schematic diagram of measurement setup: $\sigma_x = 6W(a/bh^2)$.

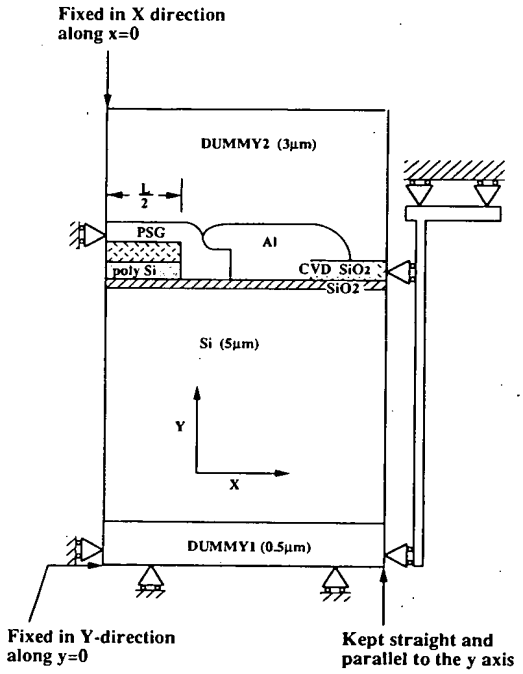


Fig. 2. Simulated device structure with the boundary conditions. The structure is the symmetry.

TABLE I
LIST OF VALUES USED FOR MECHANICAL STRESS SIMULATION

	E (GPa)	ν	$\alpha(10^{-6}/°C)$
Si [8] (poly-Si)	168	0.2	3.8
SiO_2 [8] (CVD SiO_2)	70	0.17	0.6
PSG [9]	70	0.28	4.6
Al [10]	61.7	0.34	23.2

III. EXPERIMENTAL RESULTS

A. Influence on Device Characteristics

Fig. 3 shows external mechanical stress dependence of transconductance deviation $(\Delta G_m/G_{m0})_M$ in the linear region,

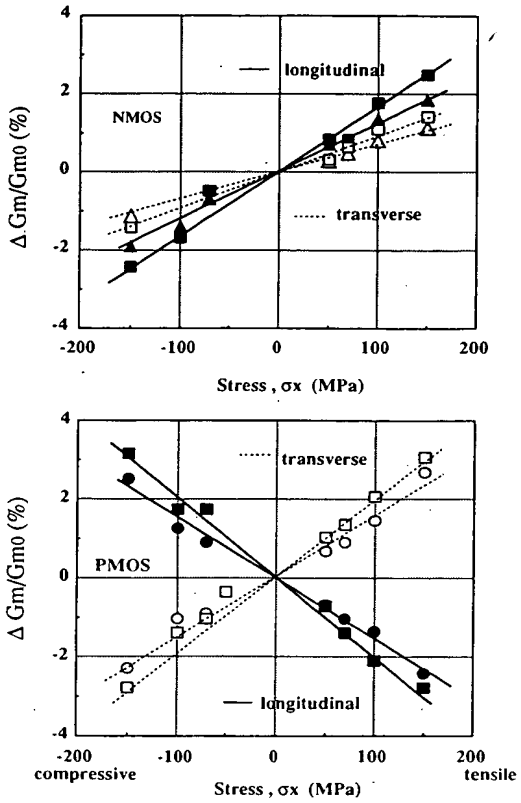


Fig. 3. Mechanical stress dependence of $(\Delta G_m/G_{m0})$ (□, ○, △: L = 2, 1, 0.8 μm).

with L as a parameter. G_{m0} is defined as a value with no external mechanical stress. For NMOS technology, as is well known, $(\Delta G_m/G_{m0})_M$ decreases under compressive stress ($\sigma_x < 0$) and increases under tensile stress ($\sigma_x > 0$) due to the pressure dependence of the bandgap [4].

For PMOS, on the other hand, $(\Delta G_m/G_{m0})_M$ decreases under compressive stress and increases under tensile stress when the stress is transverse to the current flow and *vice versa* when the stress is longitudinal to the current flow. These phenomena can be attributed to energy-level change in the valence band caused by external stress [5]. It should be noted that the slope ($(\Delta G_m/G_{m0})_M$ versus σ_x) depends on L in both NMOS and PMOS. The channel length dependence of the piezoresistance effect (PE) was reported somewhere else [6]. They deduced that process-induced stress is tensile and larger in smaller devices, and large tensile stress results in small PE. However, our simulation results is different from it as follows.

To clarify L dependence, mechanical stress distribution was simulated by imposing 10^{-4} strain in the X direction to achieve the condition of the measurements. For the first approximation, it is sufficient to take only the surface component into account because the thickness of the inversion layer is on the order of 100 Å. Apparently, the distribution of σ_x along the channel, as shown in Fig. 4, reveals the gate length dependence. The gate edge is defined as the origin and the X axis is described in units of L. For the longer channel device, σ_x concentrates at the gate edge and becomes a stable value in the middle of the channel. However, in the shorter L, no local concentrated stress component appears even at the gate edge. In addition the value of σ_x is smaller than that in the long channel. From these simulated

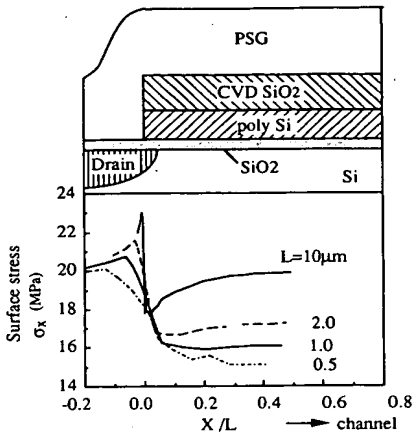


Fig. 4. Distribution of surface stress σ_x due to external tensile strain (10^{-4} strain) along the channel. $E_{si} = 1.68 \times 10^5$ MPa.

results, the stress distribution due to external stress is strongly influenced by L and this causes various device characteristics.

In order to examine the correlation between $(\Delta G_m/G_{m_0})_M$ measured electrically and σ_x calculated analytically, the gate length dependence was plotted as shown in Fig. 5. The maximum surface stress σ_x along the channel region (Fig. 4) was chosen. $(\Delta G_m/G_{m_0})_M$ was measured under a tensile stress (σ_x = 150 MPa) in the longitudinal arrangement. L dependence of $(\Delta G_m/G_{m_0})_M$ and σ_x is steeper in the region where $L < 2$ μm compared with $L > 2$ μm. That is, both $(\Delta G_m/G_{m_0})_M$ and σ_x decrease as L decreases. Furthermore, L dependence of $(\Delta G_m/G_{m_0})_M$ in NMOS begins to change at $L < 5$ μm, and it is different from that in PMOS. This difference probably results from a difference of effective mass in the electron and hole. The difference of effective mass contributes to deviation on device characteristics due to uniaxial stress; however, a further study is expected to describe this phenomena precisely. Therefore, under external stress, the L dependence of $(\Delta G_m/G_{m_0})_M$ results from the L dependence of the σ_x distribution.

An analytically vertical force was imposed on the device from the top layer, described as DUMMY2 in Fig. 2. A constant strain was assumed by using the same thermal expansion coefficient. Stress profile strongly depends on the structure and overlaid films, so the Young's modulus was chosen as a parameter to examine the difference of used overlaid films. From the simulation results, the polarity of induced surface stress depends on the Young's modulus of the top layer (E_{top}). If $E_{top} < E_{si}$, the surface stress is compressive; otherwise, if $E_{top} > E_{si}$, the surface stress is tensile. Fig. 6 shows simulated surface stress σ_x distribution along the channel using E_{top} = 100 MPa and E_{si} = 1.68×10^5 MPa. Surface stress σ_x is compressive and its value increases monotonously from the gate edge of the channel region. As shown in Fig. 7, the L dependence of the maximum σ_x along the channel shows the same tendency for all externally applied forces. Therefore, if an external force causes tensile stress at the surface, its effect on device characteristics is less in scaled devices, regardless of whether the external forces are one- or two-dimensional. However, if the external forces cause compressive stress at the surface, they begin to seriously affect reliability. This is discussed in the next section.

B. *Influence on Hot-Carrier Effect*

Surface-state density D_{it} was observed before and after bending by a high-frequency method and a quasi-static method as shown in Fig. 8. Obviously, no additional D_{it} was generated by compressive stress. Thus bending the silicon chip caused no change in the initial device characteristics in terms of D_{it}.

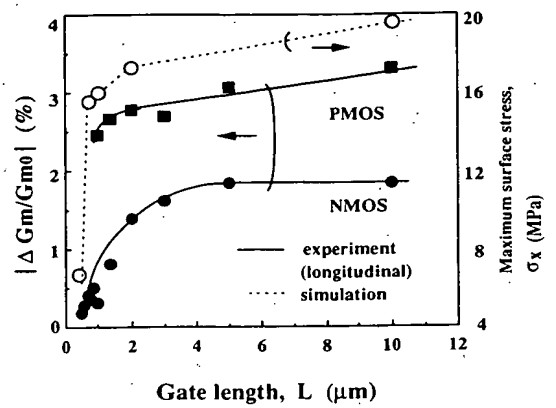


Fig. 5. Correlation between the experimental results $(\Delta G_m/G_{m_0})$ and the simulated results of σ_x maximum due to external stress.

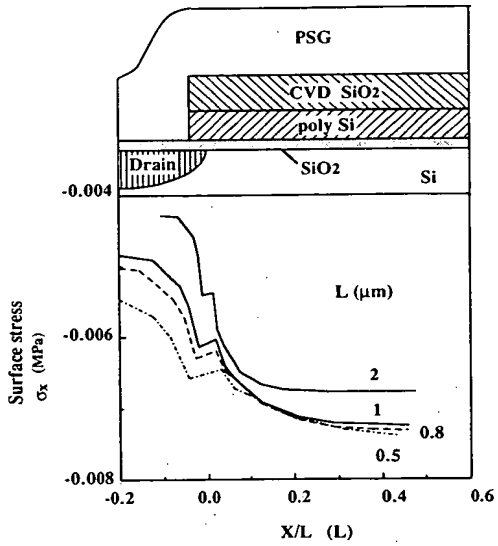


Fig. 6. Distribution of surface stress σ_x due to vertical force (10^{-4} strain) along the channel.

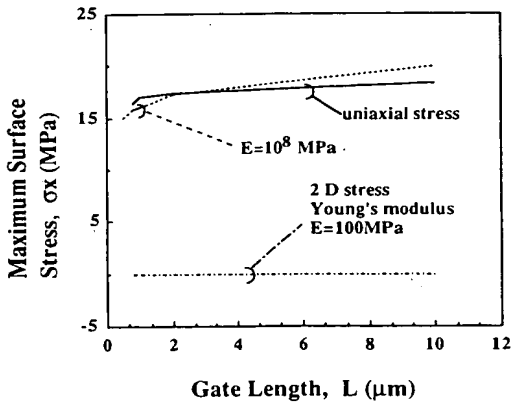


Fig. 7. Gate length dependence of maximum surface stress σ_x due to external 1D/2D force.

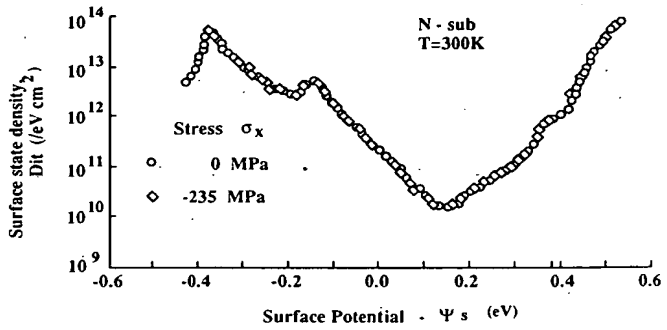


Fig. 8. Density of surface states D_{it} versus surface potential Ψ_s.

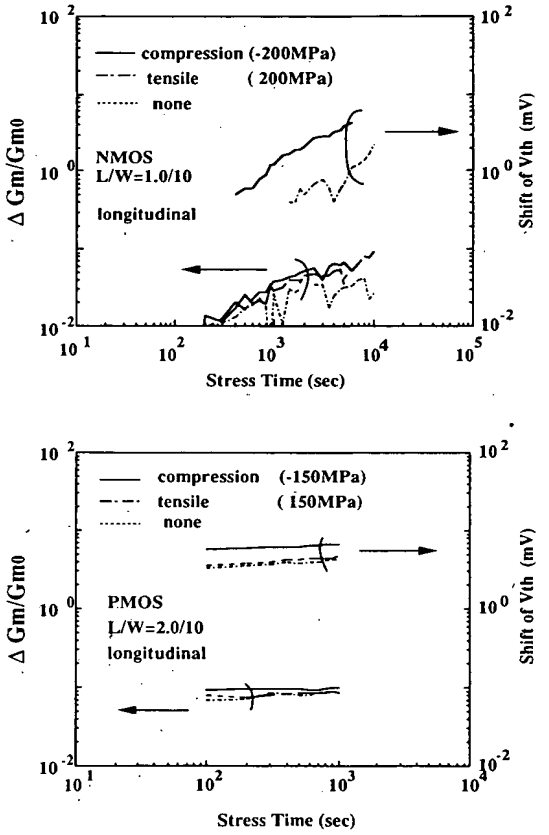


Fig. 9. Device degradation due to drain avalanche hot-carrier injection under external stress.

Fig. 9 shows the time dependence of device degradation due to drain-avalanche hot-carrier injection in both NMOS and PMOS under external stress in the longitudinal arrangement. G_m degradation was not seriously affected by the mechanical stress. However, it is obvious that ΔV_{th} is large under compressive stress for both NMOS and PMOS. The surface states induced by hot carriers are not increased by external stress. In terms of ΔV_{th}, on the other hand, the capture rate of electrons in SiO_2 is found to be greatly influenced by external compressive stress in the longitudinal arrangement. Fig. 10 shows the relationship between the surface-state density and G_m degradation ($\Delta N_{ss}/N_{ss0}$ versus $\Delta G_m/G_{m0}$), with the gate length L as a parameter, after drain avalanche hot-carrier injection. The surface-state density N_{ss} was measured by the charge pumping technique before and after hot-carrier injection for each case.

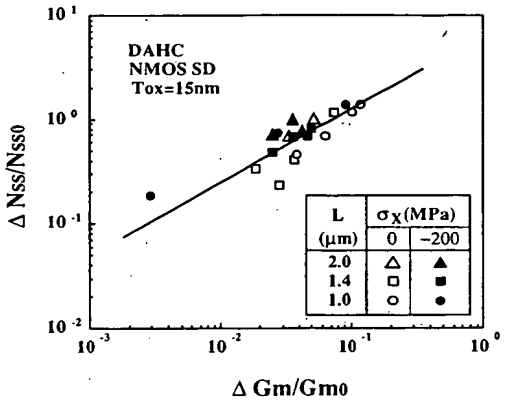


Fig. 10. $\Delta N_{ss}/N_{ss0}$ versus $\Delta G_m/G_{m0}$ after DAHC injection.

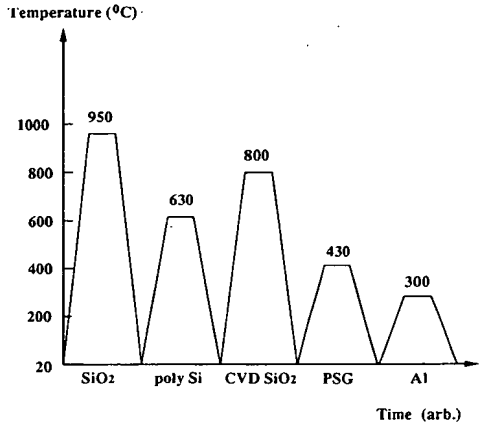


Fig. 11. Process condition for mechanical stress simulation.

ΔN_{ss} induced by hot-carrier injection can be described as a simple function of G_m degradation.

$$\Delta N_{ss}/N_{ss0} = C(\Delta G_m/G_{m0})^n, \qquad C \text{ constant}.$$

This result also implies that the mechanical stress does not affect the generation of surface-state density. From Figs. 9 and 10, even at room temperature, surface compressive strain is strongly related to the electron trapping process. Here, the bond angles of Si–O or Si–H are modulated by mechanical stress, which results in the change of the electron trapping process. However, this discussion is merely speculation.

In actuality, the stress profile induced by the thermal process is considered to affect device characteristics. A stress profile induced by thermal process was examined. In this study, the intrinsic stress was not considered. Process condition is listed in Fig. 11. Although stress σ_x is concentrated at the gate edge for $L > 1$ μm, no concentrated component appears for $L = 0.5$ μm as shown in Fig. 12. This is because in smaller devices, the restricted strength induced by the polysilicon gate is weakened. For $L = 2$ μm, a compressive component appears at the gate edge, but only a tensile component appears for $L < 1$ μm. Thus the stress distribution and its polarity strongly depend on the gate length. Fig. 13 shows σ_x distribution along the channel with L as a parameter. For the longer gate length, σ_x changes drastically at the gate edge, and for the shorter gate length σ_x changes gradually. These results are similar to those in Fig. 4. This suggests that the effects of process-induced stress on basic

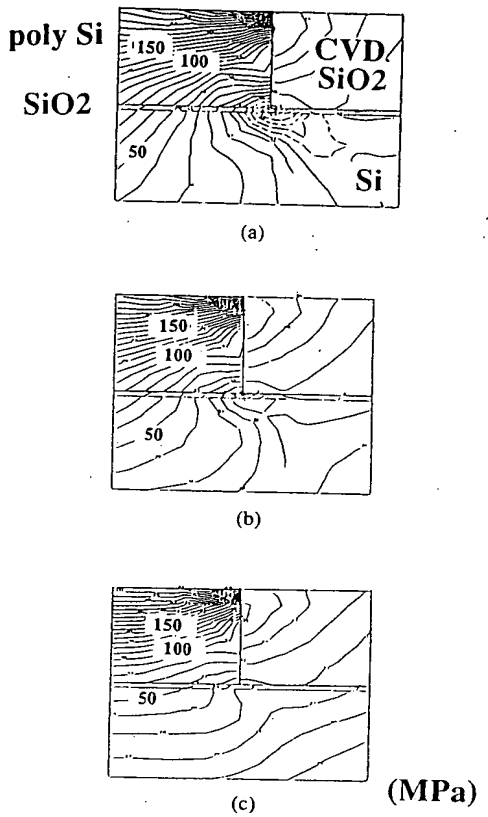


Fig. 12. Process-induced distribution of σ_x(MPa) for (a) $L = 2$ μm, (b) $L = 1$ μm, and (c) $L = 0.5$ μm.

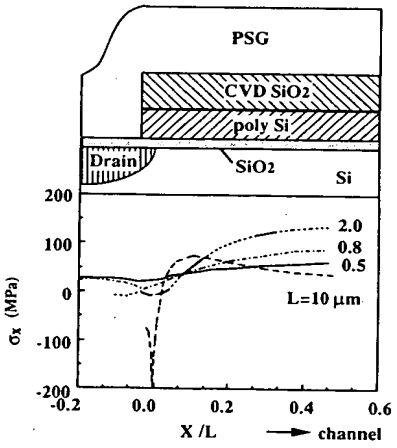


Fig. 13. Process-induced stress σ_x along the channel.

device characteristics is lower in scaled MOS devices. Fig. 14 shows σ_x distribution in SiO_2 along the channel. Only compressive stress components appeared for each gate length and the surface stress changed abruptly at the gate edge. For device reliability problems like hot-carrier effects, local stress is considered to affect device degradation because hot carriers are injected locally at the drain edge [7]. In order to consider L dependence of mechanical stress effects on hot-carrier degradation, an interface stress component, σ_x in Si and SiO_2 at 0.1 μm from the gate edge, is plotted in Fig. 15. In the silicon substrate, σ_x changes polarity as L decreases from compressive to tensile. As

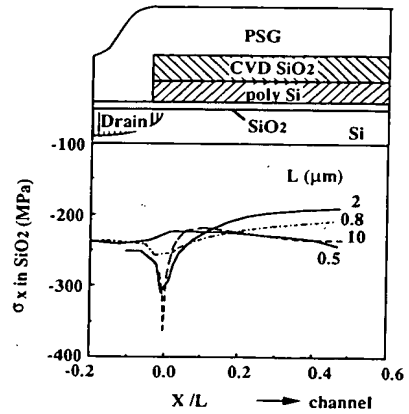


Fig. 14. Process-induced stress σ_x at the interface in SiO_2.

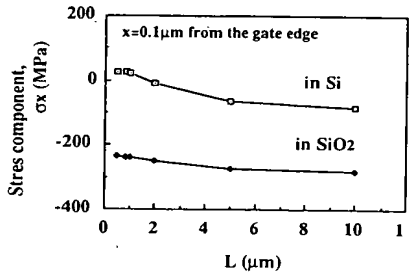


Fig. 15. Gate length dependence of σ_x at the drain edge.

mentioned above, compressive stress accelerates device degradation by hot carrier; therefore, the process-induced surface stress profile improves with scaling. σ_x in SiO_2 also decreases in value even if it is compressive. This is also a desirable direction for reliability.

IV. Conclusion

Mechanical stress effect was studied as one of the new reliability issues for deep-submicrometer MOS devices. Deviation of device characteristics due to uniaxial stress strongly depends on gate length. This results from redistribution of stress in the channel due to external stress, which is strongly dependent on L. That is, the shorter the gate length, the smaller the σ_x due to external stress along the channel. However, the simulated results suggest that if external two-dimensional forces like mold stress cause compressive surface stress, their effect becomes a serious problem in smaller devices. Thus for final fabrication processes like packaging, such an effect should be considered. Furthermore, experiments on hot-carrier injection show that external compressive stress longitudinal to the current flow increases the capture rate of electrons in SiO_2 and that tensile stress has less influence on device degradation in both NMOS and PMOS. In the deep-submicrometer devices, as long as process-induced stress under the gate is tensile, the effect on device degradation will be low. However, when it becomes compressive, much care will be necessary in process/device design.

Acknowledgment

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Mechanical Stress Induced MOSFET Punch-through and Process Optimization for Deep Submicron TEOS-O_3 filled STI Device

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Introduction

Shallow trench isolation (STI) is the key technology for deep submicron devices and begins to be used practically for advanced logic and memory LSIs. With down-scaling of device dimensions, the aspect ratio of trench increases and trench filling becomes severe even in STI structures. Therefore, choice of filling material for high aspect ratio trench is one of the important issues for deep submicron STI devices. Although the TEOS-O_3 film shows good refilling characteristics, it requires high temperature annealing in order to minimize HF etch-rate and this high temperature process results in large volume change with high mechanical stress [1]. However, the impact of this stress on device functionality and process optimization have not been investigated.

In this paper, mechanical stress induced defect generation accompanying the MOSFET punch-through in TEOS-O_3 filled STI structure is reported for the first time. This defect is located only in channel region beneath the gate oxide and causes enhanced diffusion of source/drain impurity. The residual mechanical stress of filling material and the gate electrode cause this phenomenon. Suppression of the defect generation by optimizing high temperature annealing process is also described and is verified by SRAM test vehicle.

Mechanical Stress-induced MOSFET Punch-through

The fabrication process of MOSFET with STI structure was based on 0.35μm technology [2]. The trench depth was 0.7μm to achieve 0.4μm n^+/p^+ spacing. The channel width of each transistor used in memory cell was 0.35μm and the isolation width was 0.4μm. The TEOS-O_3 film was used as a filling material to fill such high aspect ratio trenches. After CMP planarization, high temperature (≥1000°C) annealing was carried out to minimize HF etch-rate similar to thermal oxide. The gate electrode was consist of poly-Si(200nm)/WSi(100nm)/SiN(200nm) stacked structure and 100nm thick SiN sidewall was applied. In order to verify the manufacturability of this process, thousands of SRAM test vehicles (256kbit) were fabricated. As a result, it was found that some SRAM chips suffer from specific functional failure with large stand-by current more than 10μA/fail-bit. The leakage current level was higher four order of magnitude than that of junction leakage current of total active region. Moreover, the leakage current had negative temperature dependence and was same as the nMOS inverter's. These results suggest that some access transistor in cell array did not cut-off with very small probability. In fact, it was verified that an access transistor in the fail chip had large source/drain punch-through current. Therefore, it was concluded that the leakage current flew from bit-line to Vss-line through nMOS inverter consisted of access transistor and latch nMOS as shown in Fig.1. The I-V characteristic of access transistor in cell array which accompanies source/drain punch-through characteristic is also shown in Fig.2. It should be noted that this current is not a gate leakage current nor a junction leakage current of source/drain region.

Analysis

The origin of the punch-through phenomenon was studied. Figure 3 (a) shows SEM photograph of 0.35μm 6T SRAM cell after Wright etching which shows source/drain punch-through characteristics. As shown in the photograph, needlelike extended source/drain region was observed. It is considered that this enhanced source/drain impurity diffusion is caused by the defect along the channel, since the cross sectional TEM photograph reveals that crystal defects are formed in this channel region as shown in Fig.3(b). It should be noted that this defect appears beneath of the gate oxide and clearly different from the ion-implantation-induced defect at source/drain region. Moreover, this defect was observed only in access transistors and not observed latch transistors of memory cell.

In order to analyze this phenomenon, stress simulation was carried out by ABAQUS. Figure 4 shows simulated maximum Mises stress of active region of 6T cell in case that TEOS-O_3 annealing temperature was 1000°C. The channel region with concave corner shows maximum Mises stress more than 300MPa and corresponds to the region where channel defect appears as shown in Fig.3(a). Additional factor of this defect generation is the material stress of the gate electrode. There was a report about W polycide gate stress which causes dislocation in LOCOS structure [3]. As shown in the Fig.3(a), this defect was observed only access transistor region, though both access and latch transistor have concave corner. The difference between these transistors are the total gate electrode length. In the 6T cell structure, the gate electrode length of latch by nMOS and pMOS is about 3μm as shown in the cell layout of Fig.3. On the other hand, the gate electrode of access transistor (word line) was connected with more than 50 cells and its total length exceeds 100μm. From above results, it is concluded that mechanical stress by filling material and additional stress by the gate electrode material cause this defect generation in channel region.

Process Optimization

Process integration for avoiding the mechanical stress induced source/drain punch-through was also studied. The relaxation of residual stress is the fundamental solution of this problem. Since process temperature after STI formation is 800-850°C, it is important to reduce mechanical stress around this temperature. In order to minimize residual stress of the filling materials, high temperature annealing after trench filling step was investigated. Figure 5 shows temperature dependence of TEOS-O_3 film stress as a parameter of annealing temperature. By 1200°C annealing, TEOS-O_3 films stress at 850°C decreased to ≈0MPa while 1000°C annealed sample shows more than 1GPa. Annealing temperature dependence of defect density is also shown in Fig.6. As shown in the figure, 1200°C annealed sample shows defect free characteristics. The impact of 1200°C annealing on suppressing defect-induced MOSFET punch-through is shown in Fig.7. It was confirmed that TEOS-O_3 filled STI can be applied to 0.35μm 6T cell without degrading device yield by introducing optimized high temperature annealing. Moreover, simulated mechanical stress indicates that 10% size reduction in channel width increases the mechanical stress about 5% as shown in Fig.8. This result means that down-scaling of STI device dimensions in future LSIs will require careful process/material design as mentioned above for achieving lower mechanical stress and higher manufacturability.

Conclusion

Source/drain punch-through due to channel defect in TEOS-O_3 filled STI structure was found for the first time. This defect generation was caused by residual stress of filling material and assisted by the gate electrode material stress. Optimized high temperature annealing achieved defect free characteristics and enabled TEOS-O_3 as a filling material of STI structure without degrading device yield. Process integration for future STI devices should take account of this phenomenon carefully from a manufactuability point of view.

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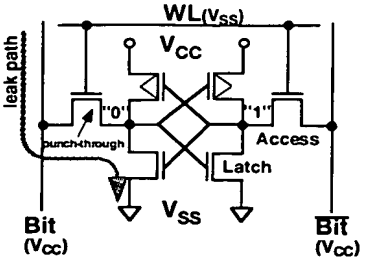

Figure 1 : Leakage current path of failed SRAM cell.

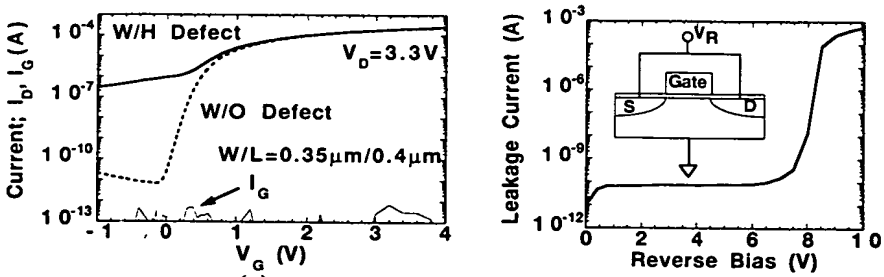

Figure 2 : (a) I-V characteristics of access transistor with and without channel defect. (b) S/D junction leakage current of access transistor with channel defect.

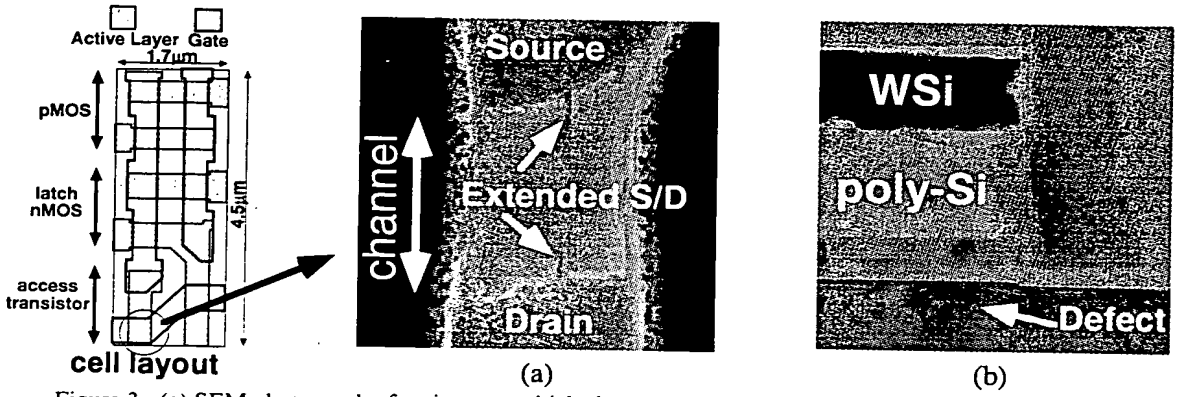

Figure 3 : (a) SEM photograph of active area which shows punch-through characteristics after Wright etch. (b) Cross sectional TEM photograph of access transistor which shows punch-through characteristics.

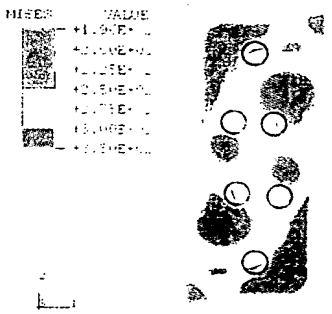

Figure 4 : Simulated maximum Mises stress of 6T cell active area. Circle mark indicate ≥300MPa stress region.

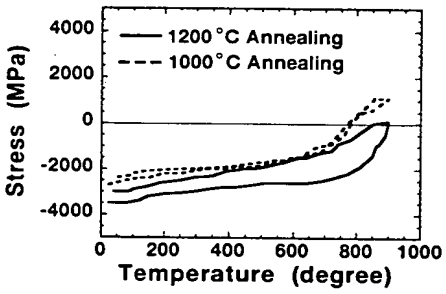

Figure 5 : Temperature dependence of TEOS-O3 film mechanical stress as a parameter of annealing temperature.

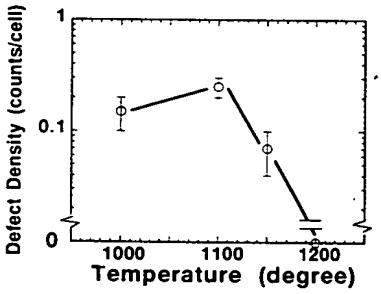

Figure 6 : TEOS-O_3 film annealing temperature dependence of defect density.

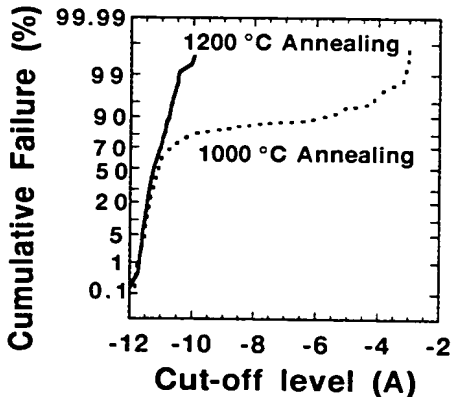

Figure 7 : Impact on high temperature annealing for defect-induced MOSFET punch-through.

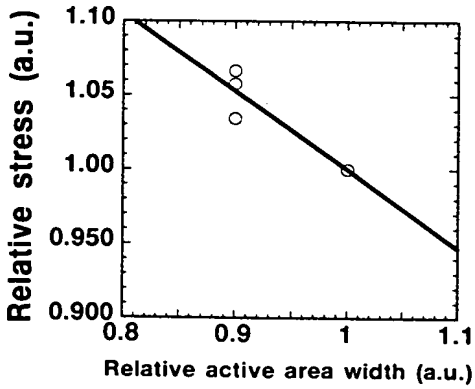

Figure 8 : Relative active area size dependence of mechanical stress.

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[4]

An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)

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ABSTRACT

Densification methods using H_2O and N_2 ambient annealing of the filled CVD oxide for quater micron STI are compared. Although the H_2O ambient oxidation is more effective in terms of the resistance against the HF etching, volume expansion by the trench sidewall oxidation generates a large amount of stress in the narrow isolation region. However, an N_2 gas ambient annealing at high temperature shows a low stress and a low HF etch rate which enable us to fabricate the stable quater micron STI.

INTRODUCTION

As a substitute for the LOCOS isolation in sub-half micron devices, STI has been challenged widely [1,2,3]. In STI, refilling of the trenches with CVD oxide using TEOS based APCVD or LPCVD have been considered as appropriate methods due to their good filling capability without forming voids. However, those CVD oxides initially have a very high etch rate in an HF solution. Proper densification, therefore, is required for the decrease in consumption of the oxide by subsequent process steps. Annealing in an H_2O ambient is known to be one of the most effective densification methods [4]. Figure 1 shows the comparison of the final profiles of the STI with and without H_2O densification.

However, a densification in the oxidizing ambient causes an unwanted sidewall oxidation, which in turn exerts an extreme stress toward the active Si area of the devices. The stress, if it surpasses the yield stress of the Si, may form crystallographic defects such as dislocations which increase the leakage current of the STI.

In this paper, the influence of the densification in the oxidizing (H_2O) and the inert gas (N_2) ambient was being compared, and the process condition for the quarter micron STI was optimized.

EXPERIMENTAL

Test structures for isolation profile observation and electrical properties were made as shown in fig.2. At first, field and active region were defined by photolithography and etch steps (fig.2 (a)). Trench sidewall oxide was grown, CVD oxide was deposited to fill the trenches (fig.2 (b)), and two densification processes were performed seperately. CMP was then applied to planarize the CVD oxide until SiN was exposed (fig.2 (c)). SiN layer was subsequently removed in phosphoric acid, and channel stop implantation was carried out. Then, the pad oxide was removed in a diluted HF solution (fig.2 (d)). Afterwards, conventional processes were performed and the junction and transistor characteristics were evaluated.

RESULTS AND DISCUSSION

Figure 3 shows the N^+/P junction leakage currents in the H_2O densification cases. At the large isolation sizes, a normal behavior with low leakage currents is obtained, but as the isolation size becomes smaller, leakage currents in low voltages begin to increase to 80 pA/cm at 4 V in 0.26 μm isolation size. Secco etching [5] of the active and field array reveals the defects with a very high density in the narrow STI, meanwhile no defects in the wide STI as shown in fig.4 are observed. This size dependency can be explained by assuming the field oxide as a visco-elastic medium. In the case of the wide field area, the field oxide is wide enough to absorb the stress caused by the areal expansion, whereas in the narrow field area, the oxide cannot hold the stress in itself and the defects are generated to release the stress.

On the other hand, fig.5 and fig.6 show the results of the CVD oxide densification in an N_2 ambient. Figure 5 shows no increase of the leakage current in the narrow field area, which means that the leakage current has no size dependency since no sidewall oxidation occurs. These clean electrical data correlate well with the Secco observations which show no defects regardless of the isolation size [fig.6]. SUPREM-IV simulations (fig.7) also verify the stress level reduction with N_2 ambient annealing.

Figure 8 compares the I_d-V_g characteristics of the transistors with three different densifications. Unlike the ones with wet oxidation and N_2 ambient at 1150 °C, devices with 1000 °C, N_2 ambient densification show hump characteristic in transistors. That is because in the 1000 °C, N_2 anneal case, the top portion of the Si trench edges (fig.10 (b)) are exposed to the high electric field of the gate during HF etch steps subsequent to the densification due to the relatively high HF etch rates of the oxides (fig.9). Meanwhile, the top corners of the Si trench are mostly covered with the CVD oxide, which prevents them from being easily inverted by the electric field of the gate both in the case of the wet oxidation and N_2 anneal at 1150 °C (fig.1 (a) and fig.10 (a)), and consequently demonstrate good transistor characteristics (fig.8).

Fully working samples of the 256 Mbit DRAM were obtained by applying the STI process with the densification in an N_2 ambient at 1150 °C.

CONCLUSION

We have compared the isolation and MOS device characteristics of the STI fabricated by the densifications of the field CVD oxide in the H_2O and N_2 ambient. In H_2O ambient, the trench sidewall oxidation generates defects at the narrow trench resulting in leaky isolation characteristics. The annealing in the N_2 ambient at 1150 °C densifies the CVD oxide efficiently without causing any abnormalities in the isolation and the MOS device characteristics.

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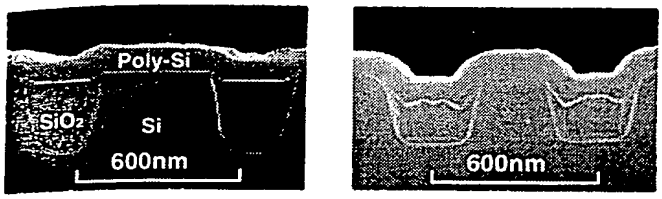


(a) (b)

Figure 1. Cross-sectional SEM micrographs of the final STI profiles (a) with and (b) without the densification. Densification was performed in H_2O ambient at 850 ℃, 30 minutes.

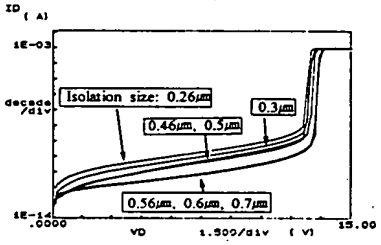


Figure 3. Junction leakage currents of the N⁺/P junction with respect to the reverse bias voltages. Peripheral length was 5.04 mm and the densification was done in H_2O ambient at 850 ℃, 30 minutes.

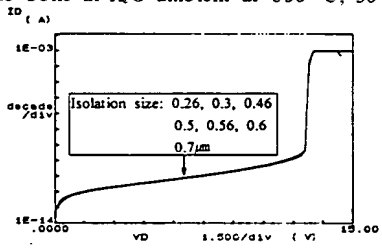
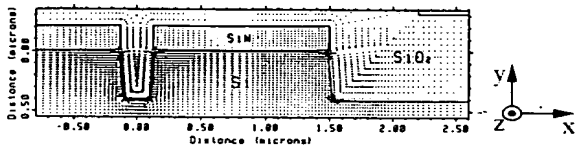
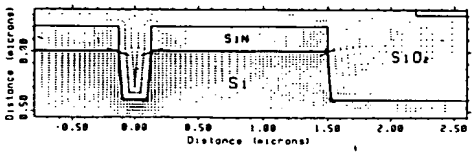


Figure 5. Junction leakage currents of the N⁺/P junction with respect to the reverse bias voltages. In this case, densification was performed in N_2 ambient at 1150 ℃, 1 hour.



(a)CVD Oxide Densification Condition: H_2O Ambient, 850℃, 30min



(b)CVD Oxide Densification Condition: N_2 Ambient, 1150℃, 1 hour

Figure 7. Stress simulations with SUPREM-IV(σ_{xx}). The darker area represents where the stress is more concentrated.

Figure 9. CVD oxide thicknesses as a function of the Bufferd Oxide Etchant (BOE) etch time in different densification conditions.

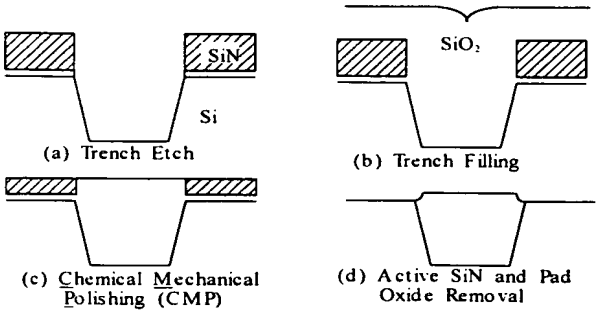
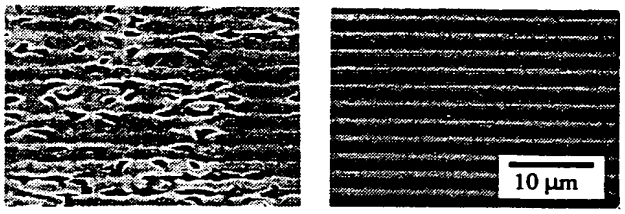
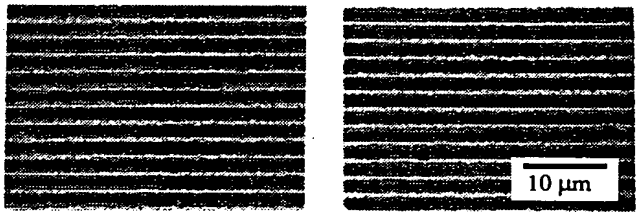


Figure 2. STI process.



(a) 0.26 μm (b) 0.7 μm

Figure 4. SEM micrographs of the Secco etched active and isolation lines. No defect is shown at wide isolation sizes whereas many etch pits which were generated by the stress in Si substrates are shown at small isolation sizes.



(a) 0.26 μm (b) 0.7 μm

Figure 6. SEM micrographs of the Secco etched active and isolation lines. No defect is shown.

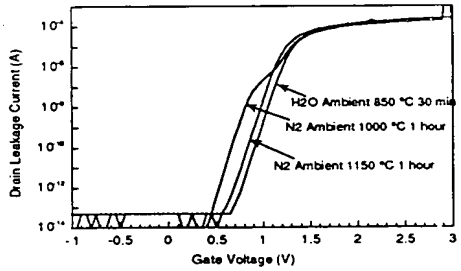
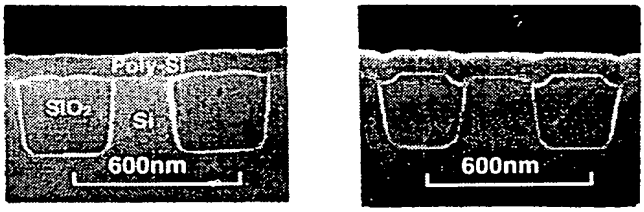


Figure 8. I_d-V_g characteristics of NMOS transistors with N_2 or H_2O ambient densification. V_d=0.1 V, V_{sub}= -3 V, W=10 μm, and L= 1.0 μm.



(a) N_2 Ambient, 1150℃ 1 hour (b) N_2 Ambient, 1000℃ 1 hour

Figure 10. Cross-sectional SEM micrograph of the final STI profile with the different CVD oxide densification conditions.

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Electrical Characteristics of Ultra-Fine Trench Isolation Fabricated by a New Two-Step Filling Process

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(Received November 7, 1996; accepted for publication November 13, 1996)

An ultra-fine trench isolation with superior electrical properties was formed using a new fabrication process. A void-free shape and sufficient thickness of the field oxide were realized by two-step filling using tetraethyl-ortho-silicate (TEOS) oxide as the lower layer and high-density CVD-SiO_2 as the upper capping layer. The breakdown voltages were as high as 7.7 V, even for an isolation space as narrow as 0.13 μm. The subthreshold characteristics of the metal oxide semiconductor field effect transistor (MOSFET) isolated by the trench were kink-free. The threshold voltage of the parasitic MOSFET, furthermore, was more than 6 V, even without a channel-stop implant to suppress punch-through.

KEYWORDS: ULSI, trench isolation, breakdown voltage, narrow channel transistor

In ultra-large scale integration (ULSI) technologies with dimensions smaller than the subquarter-micron scale, where the local oxidation of silicon (LOCOS) isolation reaches its application limit, trench isolation is expected to show its real worth due to having no significant lateral extension of the field oxide and independent controllability of its depth and width.[1] The fabrication process for a very narrow trench isolation, however, is still under development.[2–4] One of the most important steps is the oxide filling of a trench with a high aspect ratio.[5;6] Tetraethyl-ortho-silicate (TEOS) oxide is usually used in order to achieve filling without voids. The filled structure, however, has a seam at the center, which has a high etching ratio in the subsequent wet etching process, which causes an undesirable void, which may cause shorts between transistors due to the remaining gate material. Moreover, the void, which degrades the shape at the edge of the field oxide, has a significant effect on both the isolation and transistor characteristics.

In this work, we describe a new trench isolation fabrication process with two-step oxide filling by taking advantage of *soft* TEOS-SiO_2 and *hard* high-density SiO_2. The fabricated structure provides excellent electrical characteristics for both isolation and metal oxide semiconductor field effect transistors (MOSFETs), which result from the good filling shape.

Figure 1 shows the process sequence schematically. A hard mask composed of SiO_2/Si_3N_4/thermal-SiO_2 (50 nm/150 nm/15 nm) was patterned, using electron beam (EB) lithography and a dry etching technique, on a p-type (100) silicon substrate (a). The minimum isolation space (S) was as narrow as 0.13 μm. A trench about 0.3 μm deep was formed using a conventional reactive ion etching technique. After oxidation inside the trench (50 nm), the thermal oxide formed was removed by wet etching using a diluted HF solution. This step was introduced not only to eliminate the damage induced by the dry etching, but also to give the trench corner a moderate radius. Next, a fresh 10-nm-thick thermal oxide layer was formed inside the trench (b). No additional doping at the channel edges to suppress the electric field concentration was used.

The filling process starts with TEOS-SiO_2 deposition, which is followed by annealing in N_2 ambient at 900°C for 80 min. The filled TEOS-SiO_2 was selectively etched back below the silicon surface (c). Next, high-density SiO_2 was deposited by CVD as a capping layer in the trench, the aspect ratio of which had been decreased by the previous TEOS-SiO_2 filling, and was then annealed in N_2 at 900°C for 80 min.

After the surface was planarized by the etch-back (d) and the Si_3N_4 mask was removed using a boiling H_3PO_4 solution, boron implants to fabricate an n-channel MOSFET (NMOSFET) were performed. On some wafers, the channel stop implant, which suppresses punch-through between the MOSFETs, was eliminated.

The remaining thermal-SiO_2 in the hard mask was removed using a diluted HF solution (e). A 6-nm-thick gate oxide layer was grown at 750°C in O_2 and H_2 ambient. The NMOSFETs were fabricated using a conventional process together with the deposition of the polysilicon gate electrode (f).

Figure 2 shows scanning electron micrograph (SEM) cross-sectional views of trenches with S = 0.13 and 0.35 μm. For both structures, no obvious voids were observed in the centers, while moderately round trench

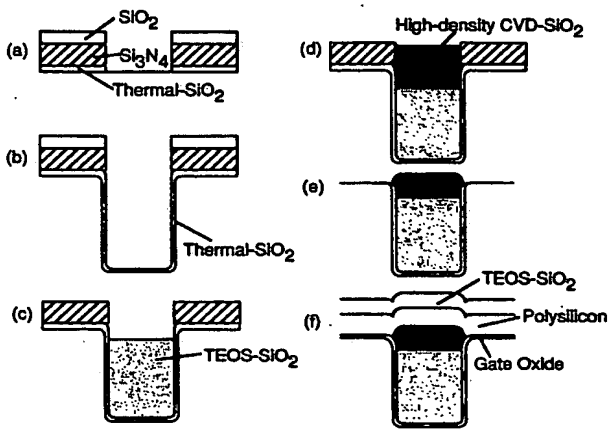

Fig. 1. Process sequence using two-step filling.

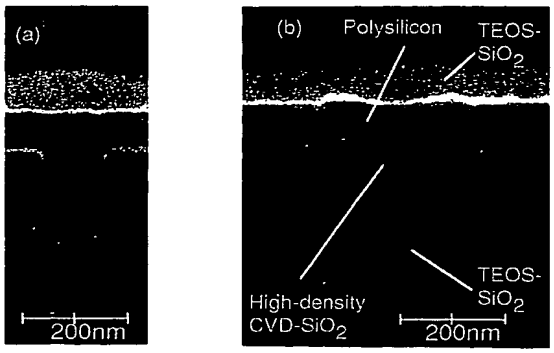

Fig. 2. SEM cross-sectional views of trenches with different isolation spaces (S): (a) $S = 0.13\,\mu$m and (b) $S = 0.35\,\mu$m.

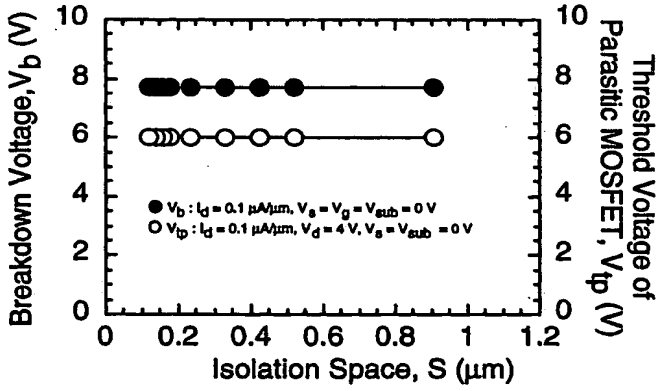

Fig. 3. Breakdown voltages of trench isolation (V_b) and threshold voltage of parasitic MOSFET (V_{tp}) as a function of isolation space (S). The maximum applied V_g was set at 6 V in order to protect the thin gate oxide.

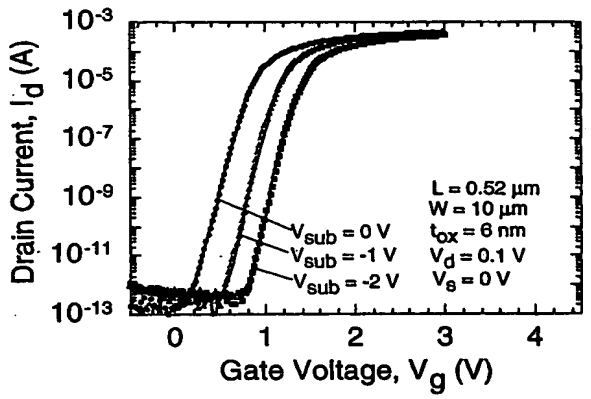

Fig. 4. Subthreshold characteristics of NMOSFETs isolated by trenches for various V_{sub} values.

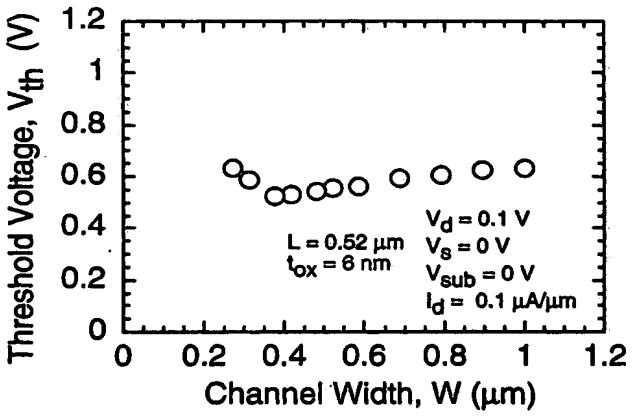

Fig. 5. Threshold voltage of NMOSFET (V_{th}) as a function of channel width (W).

edges with small side dips were obtained. These results are achieved by taking advantage of the low etching rate of the high-density capping layer as well as the reduction in the aspect ratio resulting from the use of TEOS-SiO_2, which has good conformal step coverage properties.

Next, we measured the electrical characteristics of the fabricated structures. Figure 3 shows the breakdown voltage of the trench isolation (V_b) and the threshold voltage of a parasitic MOSFET (V_{tp}) as a function of S. The maximum applied gate voltage (V_g) was set at 6 V in order to protect the thin gate oxide. V_b was defined as the drain voltage (V_d) that induces a drain current (I_d) of 0.1 μA/μm when the source, gate, and substrate voltages (V_s, V_g, and V_{sub}) are 0 V, while V_{tp} was defined as the Vg that induces $I_d = 0.1\,\mu$A/μm for $V_d = 4$ V and $V_s = V_{sub} = 0$ V. We obtained superior isolation characteristics, i.e., V_b and V_{tp} are as high as 7.7 V and more than 6 V, respectively, even for the narrow S of 0.13 μm.

The subthreshold characteristics of NMOSFETs, the channel width (W) and length (L) of which were 10 μm and 0.52 μm, respectively, and which were isolated by the trenches, were measured at $V_d = 0.1$ V for various V_{sub} values. As shown in Fig. 4, no kinks were observed even at $V_{sub} = -2$ V. That is, the electric field concentration at the trench edge was successfully suppressed. This is due to the excellent isolation structure of the sufficiently thick field oxide and the moderately rounded corners.

The threshold voltage of the NMOSFET (V_{th}) as a function of W is shown in Fig. 5. V_{th} was defined as Vg that induces $I_d = 0.1\,\mu$A/μm when $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. No significant change in V_{th} was observed. V_{th} difference between $W = 0.26$ and 1.0 μm is as small as about 100 mV. This result indicates that the present isolation is applicable to ultra-narrow NMOSFETs.

The leakage current was 9×10^{-11} A for a reverse bias voltage (V_r) of 3.6 V applied to an n^+/p^- junction (with an area of 4.216 mm^2 and an edge length of 796 mm), and the leakage current increased as V_r increased. The characteristics are comparable to those obtained using well-established LOCOS. This suggests that no significant source which enhances leakage is generated in the present process.

In addition, we report the results for wafers without channel stop implants. The leakage current was 6×10^{-11} A at $V_r = 3.6$ V and hardly depended on V_r below 10 V, while a V_{tp} of more than 6 V was maintained down to the narrow S of 0.13 μm, although V_b decreased when S reached 0.22 μm.

In conclusion, a new trench isolation fabrication technology has been developed using a two-step filling process. This process provides excellent overall electrical properties for MOSFETs as well as trench isolation. Without the use of a channel stop implant, moreover, the dependence of the leakage current on V_t decreases with little degradation in the breakdown characteristics. These excellent results indicate that the present process is promising for ULSI devices such as giga-bit scale DRAMs.

Acknowledgements

The authors would like to thank Drs. H. Abe, M. Nunoshita, S. Satoh, M. Kimata, and M. Inuishi for their encouragement and support. The authors also wish to express their thanks to Drs. T. Fujino, Y. Imanaga, A. Furukawa, K. Kanamoto, S. Yamakawa, Y. Nishioka, and T. Inbe for their technical support and discussions.

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[6]

NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress

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Abstract

This paper describes a previously unreported phenomenon wherein NMOS transistors of identical gate length exhibit a significant sensitivity to layout. Drive current may be reduced up to 13%, depending on diffusion overlap of gate. Mobility reduction, induced by stress from the trench isolation edge, is the root cause of the performance degradation. PMOS devices are not affected. Simulation results show that stress varies strongly with distance from the trench edge, and with overall diffusion size. Stress is also a major component of narrow-width effects, and explains why Idsat scaling with W differs for NMOS and PMOS devices.

Introduction

As CMOS devices continue to be scaled, effects that had once been considered secondary are becoming more important. The details of device layout, particularly the diffusion overlap of gate, have a significant effect on transistor performance. NMOS test devices drawn with relatively loose design rules may behave quite differently from transistors in an actual product, even when physical gate dimensions are the same.

Stress from the trench isolation edge is the dominant factor affecting layout sensitivity. Previous studies have shown that stress can affect device workfunction and bandgap (1), carrier mobility (2-7), junction leakage (8), and hot-electron lifetime (9). Simulation results show that trench-induced stress is of the order needed to produce the observed degradation in device performance.

Transistor Data

Transistors produced with a 0.2 µm process internally and a different process at a foundry site displayed noticeable sensitivity to transistor layout. As the diffusion size in the gate-length direction (L') was reduced to below 2 µm, Idsat dropped (Fig. 1) by 5-10%. A variety of test structures were developed to study layout sensitivity in more detail (Fig. 2): 0.2 µm transistors with small, medium and wide overlap, and wide overlap with asymmetrical gate placement. Medium-overlap transistors with different gate lengths were also included. Top-down and cross-sectional measurements confirmed that the poly dimensions of all 0.2 µm devices varied by less than 10 nm..

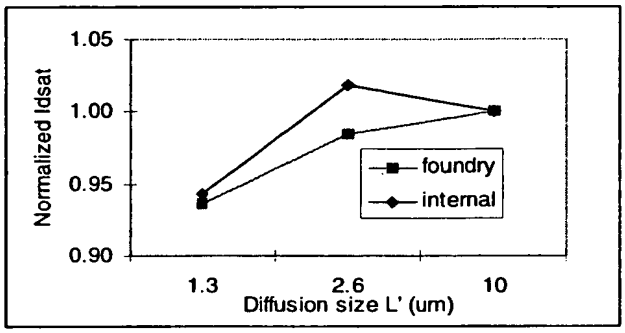

Fig. 1 Idsat vs. diffusion size in gate-length direction L' (see Fig. 2) for foundry and internal 0.2um NMOS devices. Idsat is normalized to 1 for the L'=10um device.

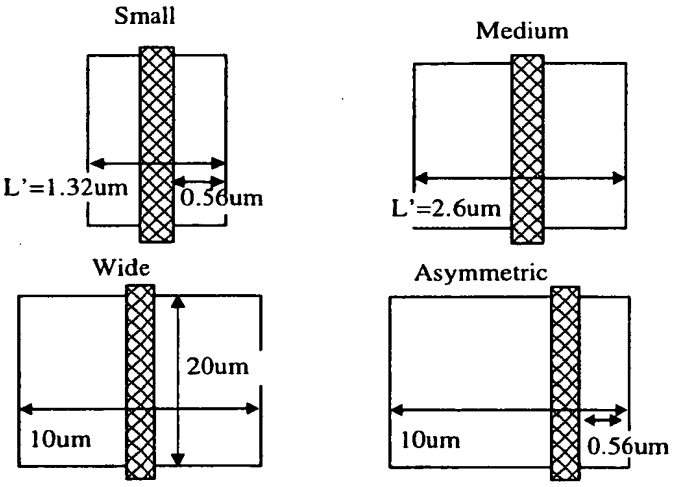

Fig 2. Layout of 0.2µm gate length transistors used in this study. All transistors were 20µm wide.

Mean Idsat of a 0.2 µm device was reduced by 7% as L' was reduced from medium to small layout, while asymmetric layout gave a reduction of 4% (Fig. 3a). The reduction in drive current seen with the small overlap corresponds to an increase in gate length of 30 nm; this is clearly a significant change. The small overlap devices also had a 25 mV increase

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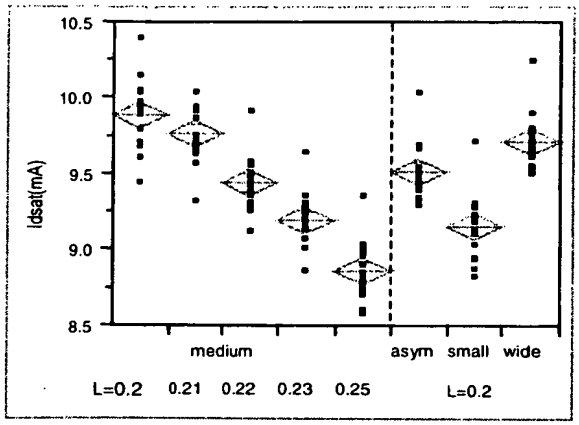
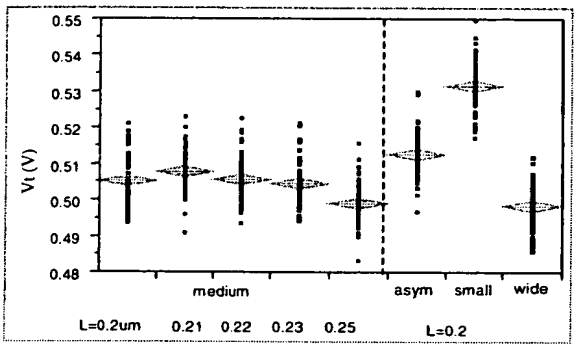


(a)



(b)

Fig 3. NMOS Idsat and Vt vs. device layout. The degradation in Idsat of a small overlap 0.2um transistor is equivalent to a 30 nm increase in gate length.

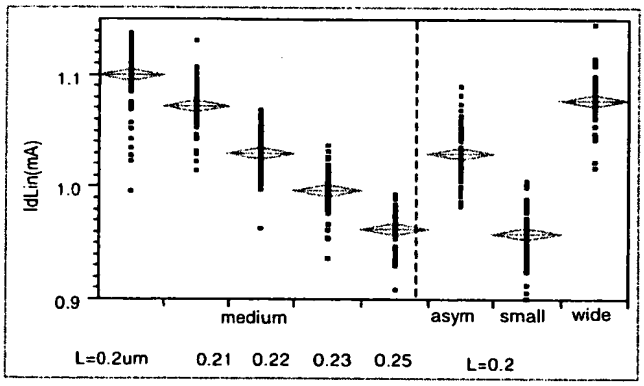
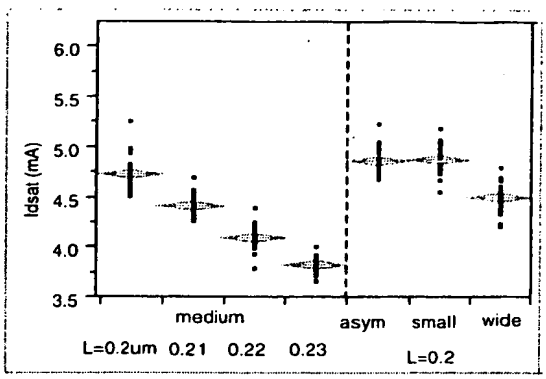
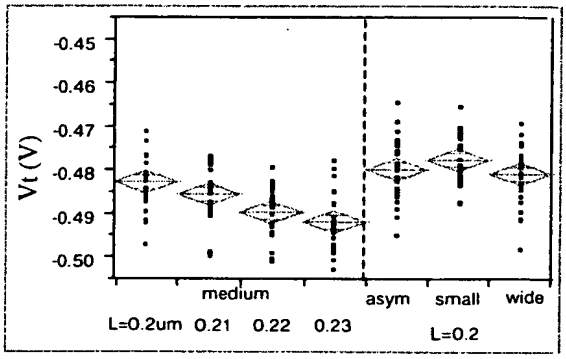


Fig. 4. Linear Id (Vg=1.8, Vd=0.05V) for different device layouts. The degradation in Id linear of a small overlap transistor is equivalent to a 50 nm increase in gate length.



(a)



(b)

Fig 5. PMOS Idsat and Vt layout dependence.

relatively small deviation

in Vt over the medium overlap device (Fig. 3b), but this Vt offset only accounts for a 2% reduction in Idsat. Linear Id (Vg=1.8, Vds=0.05V) was even more sensitive then Idsat, showing a 13% reduction as L' was reduced from medium to small overlap (Fig. 4), indicating that series resistance is not the cause of the drive current reduction. Moreover, the asymmetric device gave the same current when source and drain were reversed, arguing against an effect from silicide interfacial resistance. Proximity of the gate to the trench edge and overall diffusion size appeared to be the most significant factors. In contrast, PMOS devices exhibit little sensitivity to layout (Figs. 5a and 5b).

While the devices with various layouts had the same physical gate length, it was possible that L_{eff} differences were leading to the drive current variation. However, since L_{eff} extraction algorithms assume that mobility remains constant with varying L, we could not rely on them for this analysis. Instead, we used DIBL as a measure of the electrical channel length. DIBL measurements (Fig. 6) show that a 30nm increase in L_{eff}, which would be necessary to create the

Vt, Rsd, Leff, Mobility

34.4.2 ⇒ Leff → is almost same for all devices

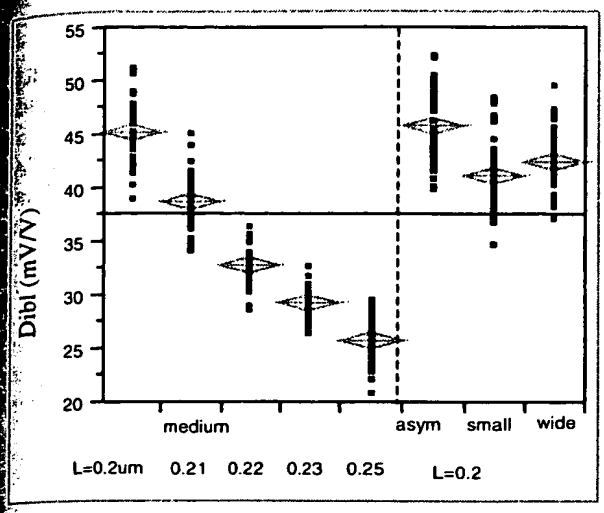


Fig 6. DIBL vs. layout type for NMOS devices. There is little difference in DIBL between 0.2um layouts, as opposed to Idsat.

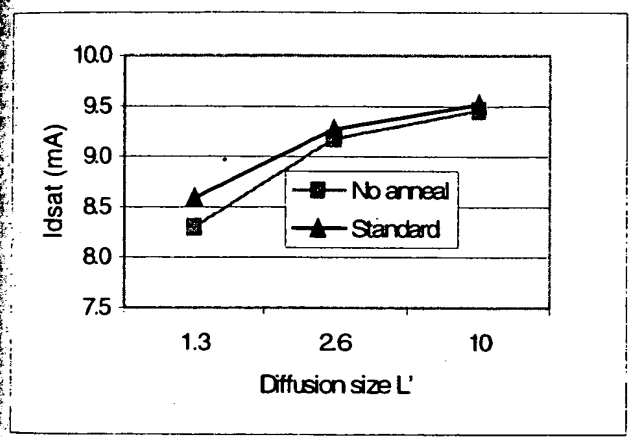


Fig. 7. Effect of no post-trench anneal on 0.2um NMOS Idsat reduction

observed reduction in drive current, would produce a 16mV/V drop in DIBL, while the DIBL offset between small and medium overlap devices was less than 4mV/V. This indicates that L_{eff} is essentially the same for all transistor layouts.

The only reasonable explanation for the drive current reduction is mobility degradation. Literature data indicates that compressive stress in silicon, through the piezoresistive effect, causes a reduction in electron mobility, while it has a minimal effect on hole mobility (3,4). Therefore, NMOS devices will be affected more by trench stress than PMOS, as we have observed. To further verify this model, wafers were processed without a post-trench-anneal step, which is known to increase stress in the silicon. As expected, NMOS devices

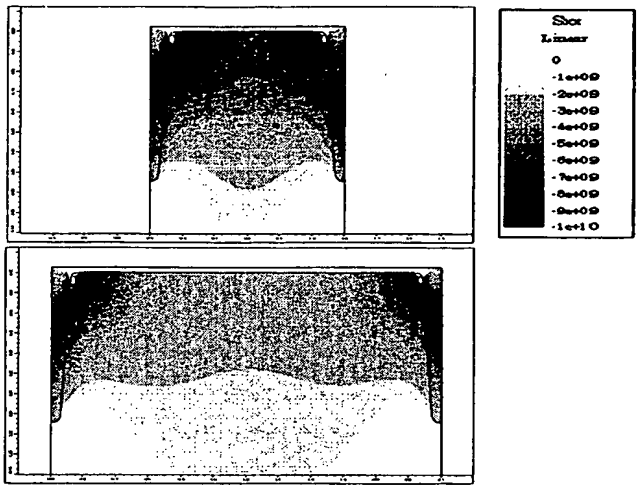


Fig 8. Stress simulation of small and medium overlap transistors

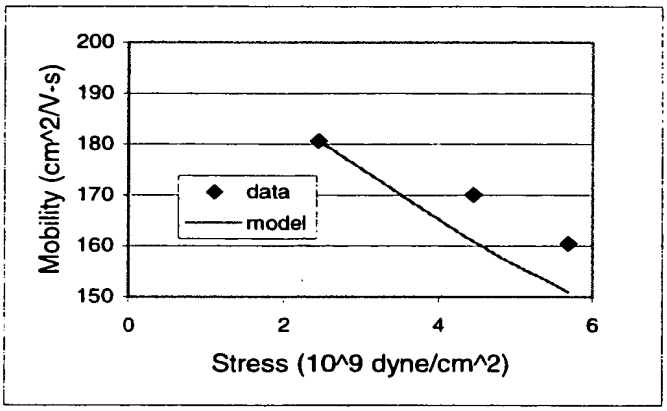


Fig. 9. Mobility dependence on simulated stress

processed without the anneal showed even greater sensitivity to the transistor layout (Fig. 7).

The change in Vt between large and small overlap devices was greater for high-Vt transistors, which have more boron in the channel. This indicates that stress-enhanced diffusion (10) is one factor contributing to the Vt offset.

Simulation Results

SUPREM simulations show that stress in the diffusion area varies strongly with the size of the diffusion, increasing from 2.4 to 5.7×10^9 dyne/cm^2 as L' shrinks from 2.4 to 1.2um (Fig. 8). Further simulations show that the asymmetric layout creates a stress of 4.7×10^9 dyne/cm^2 under the gate. Plotting

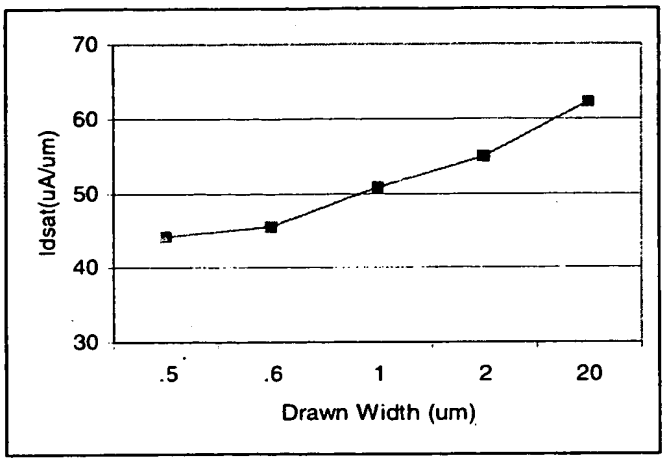


Fig. 10. Idsat (μA/μm) of L=2μm NMOS devices of various widths. The gate overdrive (V_g-V_t) was normalized to eliminate the impact of Vt rolloff.

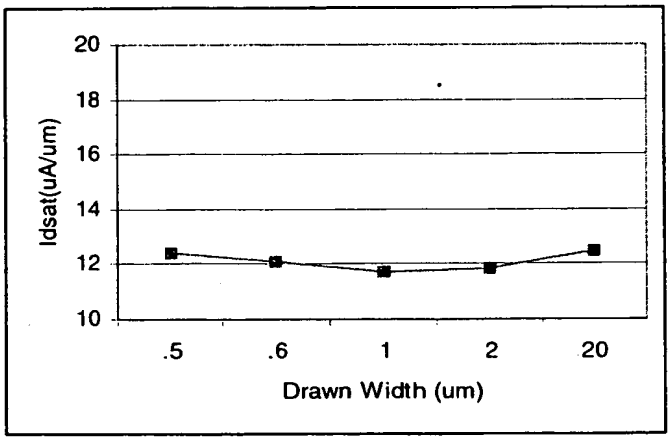


Fig. 11. Idsat (μA/μm) of L=2μm PMOS devices of various widths. The gate overdrive (V_g-V_t) was normalized to eliminate the impact of Vt rolloff.

electron mobility extracted from linear current measurements as a function of simulated stress (Fig. 9), we observe qualitative agreement with simple calculations based on the piezoresistance model.

Narrow Devices

Narrow NMOS devices also exhibit Idsat reduction as the width is decreased. Fig. 10 is a plot of Idsat vs. device width for L=2μm transistors. We chose longer channel devices to avoid complications of short-channel effects and velocity saturation. Reduction in Idsat is normally modeled by an effective-width decrease. However, there is essentially no trench encroachment in this case. Moreover, PMOS devices are not affected over this range of W (Fig. 11). The same stress-dependent mobility phenomenon described above appears to be operating here. The highly stressed region near the trench edge becomes a greater fraction of the total device width as W decreases; stress in the center of the active region increases at the same time.

Summary

We have shown that mobility reduction due to stress from trench isolation makes NMOS drive current highly sensitive to transistor layout. Trench stress is also a major component of narrow-width effects, and helps to explain why NMOS and PMOS devices behave differently as W is scaled. These effects will increase as design rules are shrunk for future generations.

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[7]

Elimination of stress induced silicon defects in very high-density SRAM structures

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Abstract

Silicon defects induced by excessive mechanical stress are correlated to leakage current and yield loss in very high-density 0.18µm SRAM devices. A specifically designed test structure, highly sensitive to strain and defects, is used for a quantitative understanding of the mechanisms responsible for the stress generation and statistically evaluate the experiments and process changes set in order to relieve the silicon defects. Hence, the elimination of the silicon defects is obtained with a minimum set of changes in the process flow, leading to a drastic yield improvement in these very dense SRAM devices.

1. Introduction

Stress induced silicon defect have been largely reported as one of the major issues in IC fabrication processes [1-2]. The extensive use of STI (Shallow Trench Isolation) associated with increased density and reduced feature size leads to critical designs for mechanical strength. The thermal treatments as well as implantations are also recognized to be the source of localized stress and silicon defects [3], which evolve into leakage current, and dysfunctional devices.

The difficulty in facing such dislocation problems is to get rapid, quantitative and complete statistical response to process variations and performed experiments. TEM and SEM with specific delineation observations do not give statistical conclusions. Yield on specific devices such as SRAM does not provide a quicker enough response. In this work, using a specific test structure, we electrically demonstrate the effect of cumulative stress induced either by successive oxidations and deposited films intrinsic stress. A mechanism for circuit failure, due to dislocation occurrences, is proposed and

Figure 1: Dislocations observed in the SRAM devices by TEM cross-section; two types of crystal defects are observed: deep dislocation between two STI bottom corners and surface dislocations crossing active S/D junction.

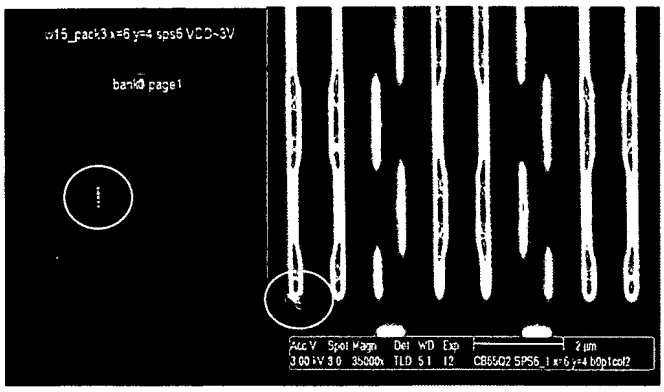

Figure 2: Correlation between photo-emission performed on SRAM array blocks and SEM observations proving that the failing mode is related to the dislocations. Highlighted circles show the hot spot and the dislocations in exactly the same columns

experimentally verified. Perfect correlation to SRAM consumption current and yield is obtained.

2. Experimental observations and discussion

Dislocations have been observed in 0.18µm specific designs of dense SRAM (diffusion ROM and 8.5µm2 dual port SRAM), using 20sec Aragona delineation and SEM observations. They impact only NMOS transistors and appear at RTA after S/D N+ implantation. Using top view and cross section TEM, two types of dislocations have been identified: dislocations running from the silicon surface down to the STI bottom corner and dislocations across two STI bottom corners (figure 1). A good correlation between leaky cells and dislocations was obtained (fig. 2).

The process sequence includes a 3500A deep STI, filled with densified TEOS, a 100A sacrificial furnace oxidation prior well implantations and two gates oxides thickness. Gate stack is formed with 2000A amorphous silicon. Following the TEOS/Si3N4 spacers formation, a heavy As implantation is performed to build the N+ Source Drains.

In this process flow, several steps have been suspected as main contributors for dislocation generation: first the STI formation, oxidations and gate deposition, each contributing to cumulative high stress fields in the substrate; secondly, the S/D implantations, which are known to induce large silicon damages and point defects contributing to dislocations nucleation and glide [4-5].

Then, experiments have been focused into these critical steps. Dislocations were physically analysed with HF + Aragona deprocessing and SEM observations, but also electrically, at metal 1 level (M1) with an original test structure, which allows rapid and complete statistical results. Figure 3 shows the layout of the RAM-cells-based test structure

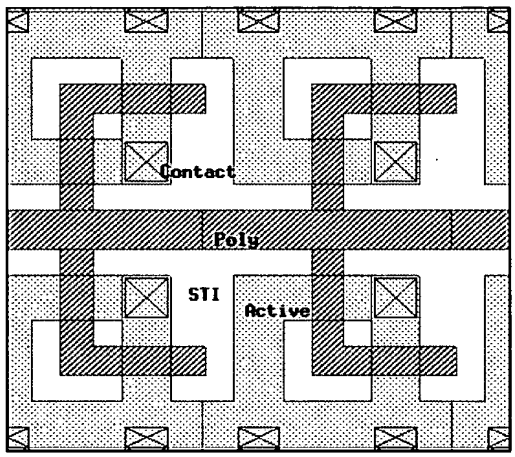

Figure 3: Layout of the RAM-cell-based test structure. Currents (Id, Is, Ig and Ib) are measured at M1 with and without back-bias.

specifically designed to be highly sensitive to dislocations and testable at M1 with simple leakage test pattern. Correlations between M1 tests on this test structure, Aragona Deprocessing, final current consumption test and yield on SRAM devices was done in parallel to ensure a good confidence in the M1 test conclusions.

In the first experiments, (fig. 4), as expected, we observed that dislocations induced current leakage measured at metal 1 decreased with the STI depth. However, the process remains marginal since, even with the shallowest STI, some leaky sites are still observed. With further decrease (2300A depth),

isolation between devices is no more guaranteed due to a too much shallow STI thick oxide.

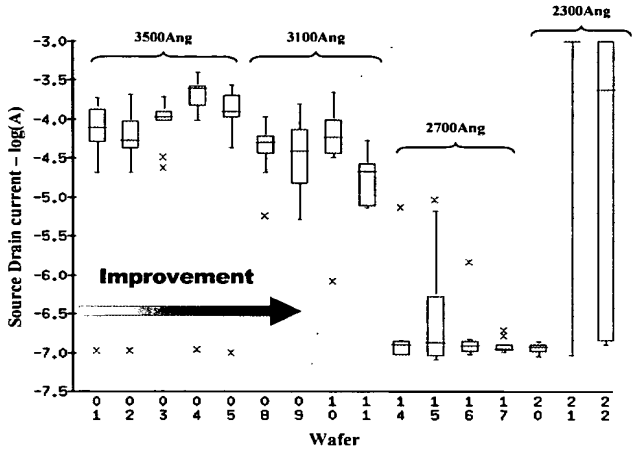

Figure 4: Source to drain leakage current decrease with STI depth. Best compromise between leakage due to dislocations and isolation efficiency is obtained with 2700 Angs. However some leaky point remain

Optimising the oxidations budget and

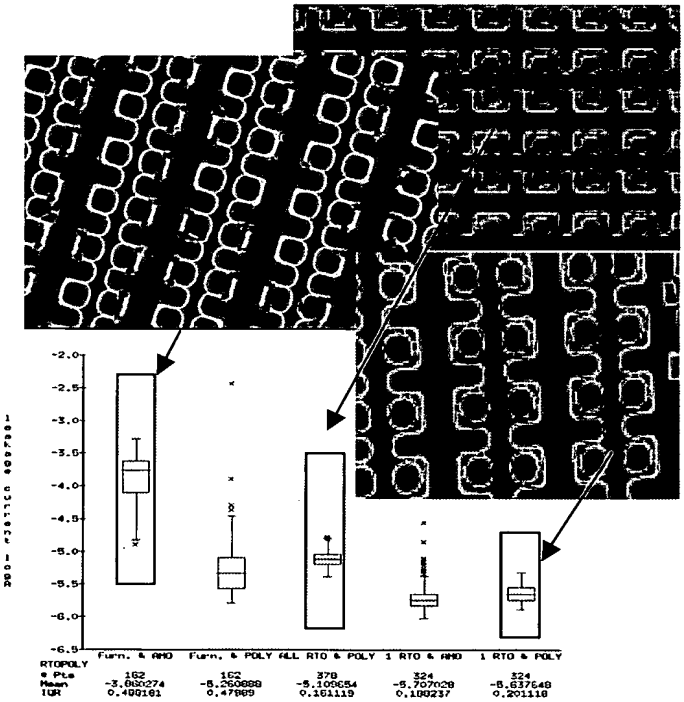

Figure 5: Impact of gate material intrinsic stress and oxidation induced stress. Using polysilicon and RTO is efficient to remove all dislocations and eliminate leakages.

changing the intrinsic stress in the gate material allowed us to reduce the final stress field, and consequently the leakage current (see figure 5). With a polycrystalline deposed poly-silicon gate, instead of the standard amorphous film, the leakage current is strongly reduced. Drastic reduction is also obtained using a wet RTO process (In Situ Steam Generation process) for the 100A sacrificial oxidation. This process avoids STI edge reoxidation, by eliminating the diffusion of oxidant agents through the STI edge. When a furnace oxidation is used, the volume expansion associated with this edge reoxidation generates very high stress at top STI corners, which then contributes to the dislocation glide. Combination of these two process changes is shown to be a robust solution, since no maverick leaky points are measured within more than 300 sites and no more dislocations are seen with extensive SEM observations. Using a wet RTO process for the gate-oxide oxidations is also efficient for stress reduction, but it represents a major change for an already optimised technology.

Experiments have also been carried out in order to eliminate the silicon damages, which are supposed to nucleate the dislocations.

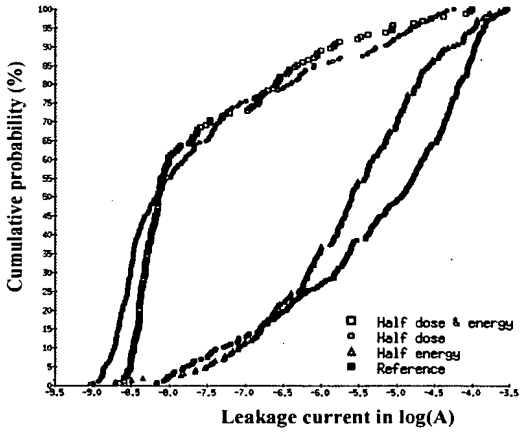

Figure 6: Cumulative probabilities of S/D leakage for different S/D implantation conditions (Dose and energy). Reducing Arsenic dose leads to good improvement

Firstly, dose and energy of the N+ source drain implantation have been decreased to generate less damage. Secondly, low temperature and long time (>4h) furnace anneals was done after

arsenic source drain implantations in order to restore the silicon crystallinity and eliminate main point defects. Figure 6 shows that the density of defects is significantly reduced with a dose divided by a factor 2, whereas energy seems to have less impact. This is in agreement with previous published work [6], and is consistent with the hypothesis that Arsenic implantation is largely responsible for the defects generation that can lead to dislocations when located in stressed silicon.

Surprisingly, experiments trying to restore the silicon damages with different low temperature anneals seem not to be efficient: no evident improvement is observed within the different temperature and time variations. However anneal ambient seems to have some impact since a slightly oxidant anneal (3%O2) gives the best improvement in this experiment (fig 7).

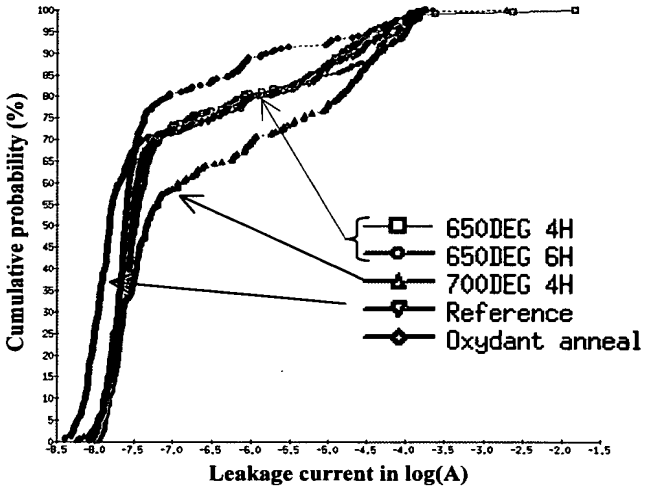

Figure 7: Cumulative probabilities of leakage current with an additional low temperature. Different process conditions are investigated; Reference process has no extra anneal

Based on all these experimental results the process flow has been optimised, changing the minimal number of critical steps. Sacrificial oxidation has been changed from furnace to wet RTO process and gate from amorphous to poly-crystalline deposed poly-silicon film. Critical SRAM devices have been manufactured with the new process, showing huge yield improvement and low static current consumption. Figure 8 shows the yield improvement for the most sensitive SRAM designs.

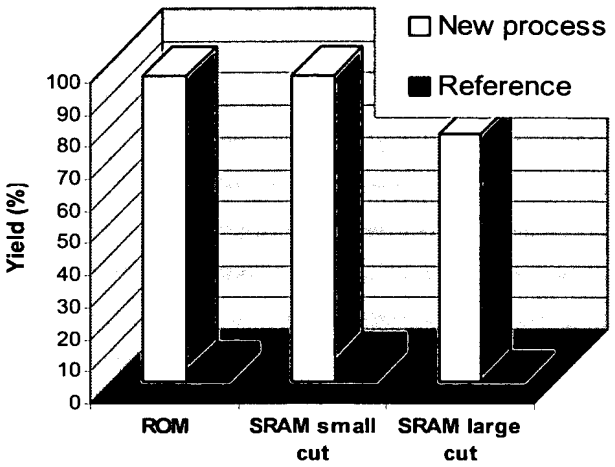

Figure 8: Yield on 3 SRAM devices reached with the optimised process flow (SACOX RTO and poly-crystalline deposed poly-silicon film), compared with the reference process

6. Conclusion

Silicon dislocations were observed in 0.18µm very high-density SRAM. Based on physical and electrical analysis using an original test structures, the key process steps have been identified and optimised, with minimal impact on the overall technology. Reducing the oxidation budget, using wet RTOs, and the intrinsic stress of gate material was the ultimate solution for a dislocation free process.

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Accurate Modeling of Trench Isolation Induced Mechanical Stress effects on MOSFET Electrical Performance

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Abstract

A new approach is presented aiming at modeling mechanical stress effects which impact MOSFET electrical behavior. It shows successful in accounting for mobility variations experimentally evidenced on complex MOSFET geometries. The newly developed mobility model proves to be an efficient way to include mechanical stress effects into standard simulation models. We show that stress effects can and should be taken into account in the IC design phase in present and sub 90nm nodes CMOS generations.

Introduction

CMOS devices down scaling demands an increasing complexity in modeling to take into account new effects impacting MOSFET electrical behavior due to the ever increasing density of integration. Shallow Trench Isolation (STI) induced mechanical stress is the dominant source of mechanical stress variations in MOSFET channel following MOSFET geometry variations, such as Active Area (AA) size & shape, gate location inside AA, etc. It may account for more than ±15% mobility variations (see Figure 1).

Other authors have evidenced this phenomenon [1]. Better understanding has been strived for aiming at controlling and reducing the stress [2] [3].

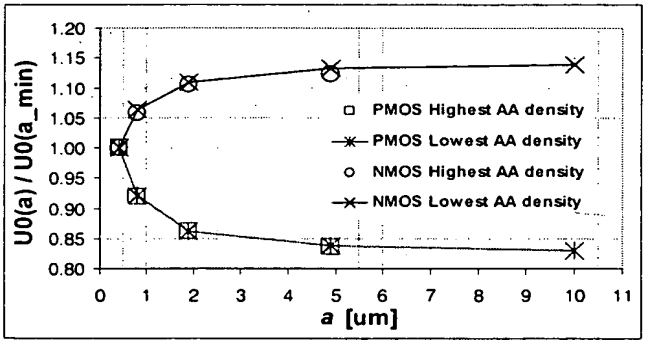

Figure 1. Measurement of low-field mobility variations versus AA size, showing opposite behavior according to MOSFET channel doping.

The originality of the present work is instead to get around its deleterious effects, and potentially take advantage of the phenomenon, by accurately accounting for stress effects in simulation models. The approach is based on mechanical simulations, test structures design and tests, performed on 0.12µm and 0.18µm CMOS technologies, to extract phenomenological laws to be implemented in simulation models delivered to designers.

Mechanical Simulations

Former work [4] allowed an estimation of stress evolution along the process flow. Based on ANSYS FEM simulation, we now focus on the STI contribution to in-plane stress variations according to MOSFET shape.

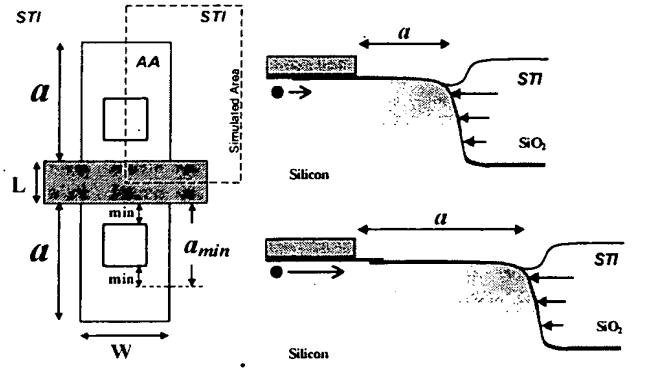

Figure 2. Standard shape MOSFET (rectangular AA and centered gate) planar & cross section views (a_{min}: minimum "a" including a single contact row).

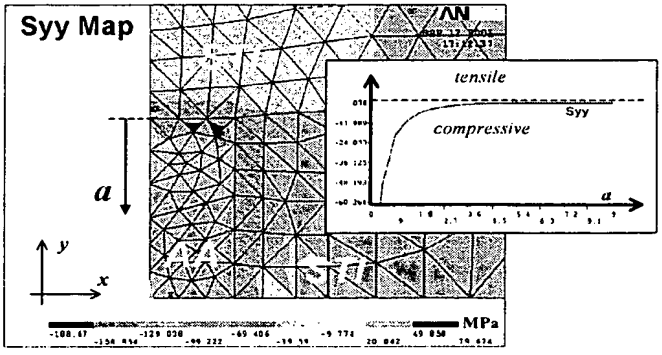

Figure 3. Mechanical simulation of Syy stress on the upper-right quarter of a rectangular AA (dashed frame area in Figure 2). Along "y" axis, compressive stress decreases when "a" increases.

Here the simulated process is limited to a 1000°C ramp down from a high temperature relaxed viscous state towards ambient state of the STI oxide. The geometrical model is limited to a two-material oxide/silicon pattern in 3D. Due to a difference in thermal expansion coefficient between silicon and silicon-oxide in the STI, a compressive state of stress develops as a peak at the AA-STI interface. The level of local compressive stress "Syy" attenuates as a function of distance to the STI edge "a" as shown in Figure 3, and according to the following model:

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$$Syy(a) = Syy(a_{min}) \cdot \left[1 + Vm_{Syy} \cdot \left(\frac{a - a_{min}}{a}\right)\right] \quad (1)$$

where an "a_{min}-MOSFET" is taken as a reference (see Figure 2) and "Vm_{Syy}" represents the maximum Syy(a) variation (i.e. when $a \rightarrow \infty$) with respect to Syy(a_{min}), as shown in Figure 4 and Figure 5.

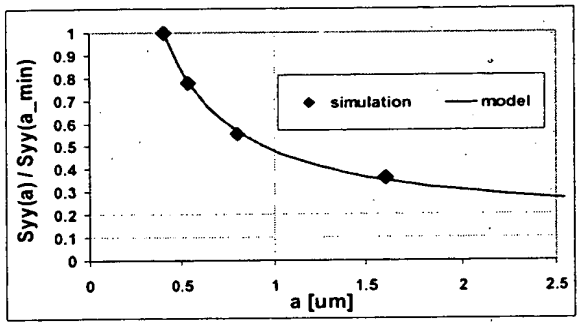

Figure 4. Evolution of simulated Syy stress at the center of the channel with respect to AA size.

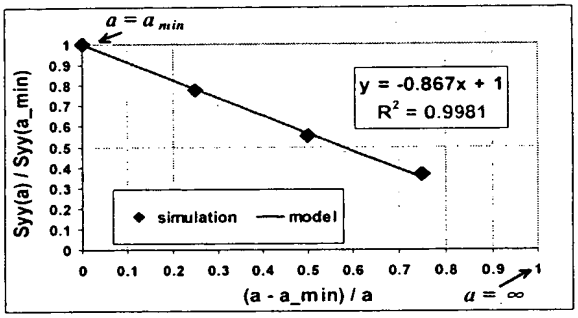

Figure 5. Simulated Syy stress and linear model fitting.

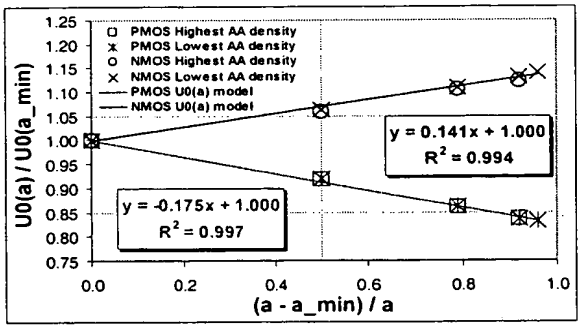

Figure 6. Measurement of low-field mobility variations, and linear model fitting, performed on NMOS and PMOS transistors of various sizes and densities.

Phenomenological Low-Field Mobility U0(a) Model

Assuming a linear relation between low-field mobility U0 and Syy variations, equation (1) form can be successfully used to model U0(a) too:

$$U0(a) = U0(a_{min}) \cdot \left[1 + Vm_{U0}(W,L) \cdot \left(\frac{a - a_{min}}{a}\right)\right] \quad (2)$$

$Vm_{U0}(W,L)$ is the maximum U0(a) variation with respect to U0(a_{min}), which is quite W-independent but is increasing for decreasing L (see Figure 7). Consequently, L and a_{min} down scaling in future advanced CMOS technologies may lead to even more pronounced stress effects on mobility. Figure 6 shows a very good fit between experimental data and model as well as no significant AA density effect.

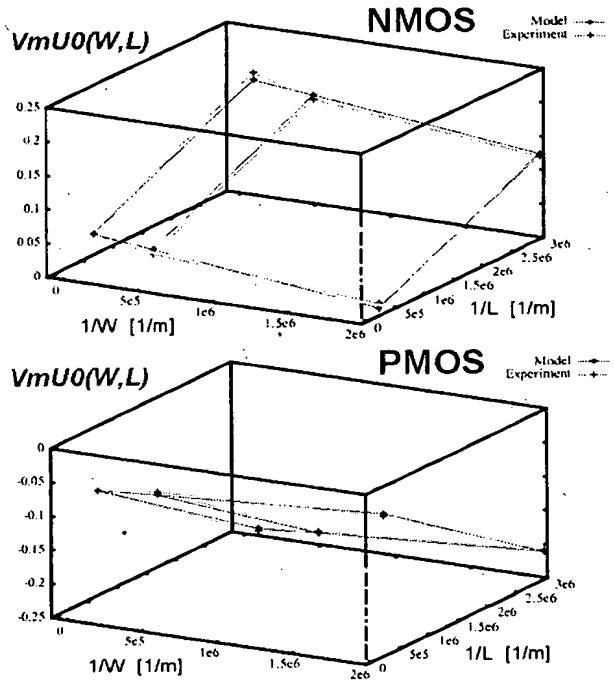

Figure 7. Experimental data and interpolation surfaces of maximum mobility variation $Vm_{U0}(W,L)$. Both NMOS and PMOS $Vm_{U0}(W,L)$ are rather W-independent and they increase with decreasing L.

Irregular MOSFET shapes

The aim is to extract an equivalent gate-to-STI distance "a_{eq}" from any irregular MOSFET shape, so that equation (2) model can be applied.

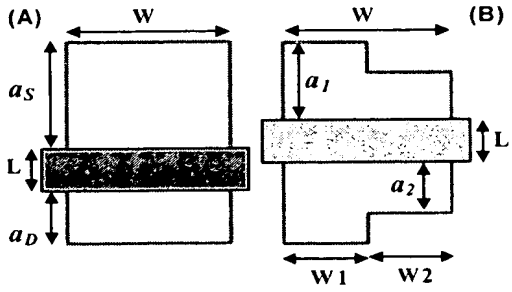

Figure 8. Asymmetric (A) and Composite (B) MOSFET shapes.

❑ To address asymmetrical MOSFET shapes (i.e. $a_D \neq a_S$, see Figure 8) we isolate in (1) the respective source and drain side contributions to stress variation, to obtain the

expression for the equivalent distance to STI "a_{eq}", as follows:

$$\frac{Syy(a_{eq})}{Syy(a_{min})} = 1 + \frac{Vm_{Syy}}{2}\cdot\left(\frac{a_S - a_{min}}{a_S}\right) + \frac{Vm_{Syy}}{2}\cdot\left(\frac{a_D - a_{min}}{a_D}\right) \Rightarrow \frac{1}{a_{eq}} = \frac{1}{2a_S} + \frac{1}{2a_D} \quad (3)$$

❑ We assume the composite MOSFET in Figure 8 to behave as two independent shunt standard-shape MOSFETs. Taking into account the total mobility U0(a_{eq}), at any conduction regime, and equation (2), we obtain the following expression for the equivalent distance "a_{eq}",

$$U0(a_{eq}) = \frac{U0(a_1)\cdot W_1 + U0(a_2)\cdot W_2}{W} \Rightarrow \frac{1}{a_{eq}} = \frac{W_1}{W\cdot a_1} + \frac{W_2}{W\cdot a_2} \quad (4)$$

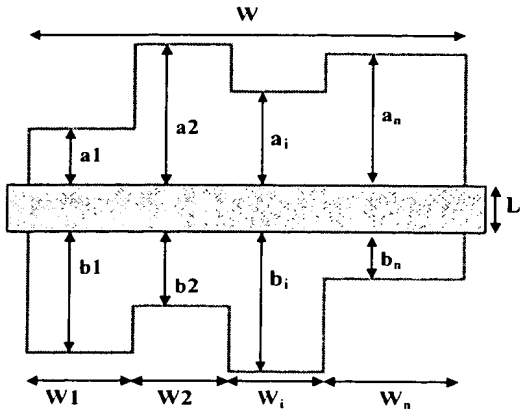

Figure 9. General shape MOSFET planar description.

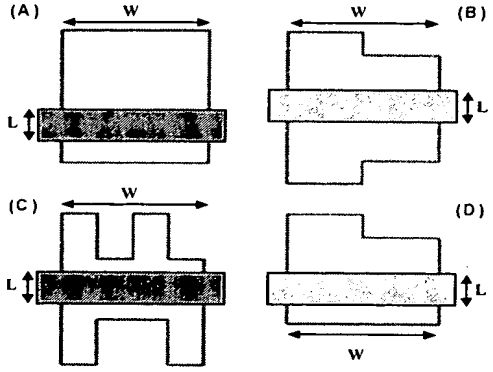

Figure 10. Tested irregular shape MOSFETs.

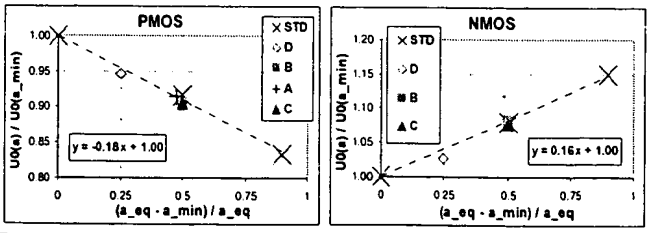

Figure 11. Mobility measurements of irregular shape MOSFETs (see Figure 10) compared to standard shape ones (STD) and U0(a_{eq}) model. Both standard and irregular shape MOSFET mobility variations can be described by the same model.

❑ The general MOSFET shape in Figure 9 can then be modeled by (2) replacing "a" by "a_{eq}", the latter being computed with the following expression, obtained from (3) and (4),

$$\frac{1}{a_{eq}} = \sum_{i=1}^{n}\frac{Wi}{W}\cdot\left(\frac{1}{2a_i} + \frac{1}{2b_i}\right) \quad (5)$$

The low-field mobility U0 of irregular shape MOSFETs in Figure 10 have been tested and compared to standard shape MOSFETs and to U0(a) model, by means of "a_{eq}" calculation. Figure 11 shows that both standard and irregular shape MOSFET mobility variations can be described by the same model: U0(a_{eq}) according to respectively (2) and (5).

STI Induced Stress versus Cobalt Silicide Stress

In the past, stress effects with respect to AA size have been attributed to Cobalt Silicide ($CoSi_2$) formation process on Drain/Source regions [5], and the need for lower stress $CoSi_2$ processes has been suggested.

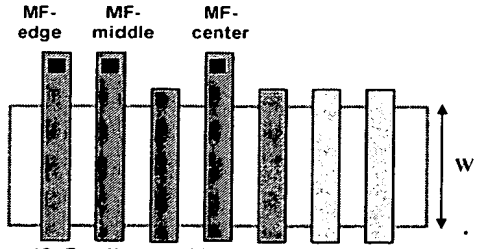

Figure 12. Equally spaced Multi-Finger (MF) shape MOSFETs.

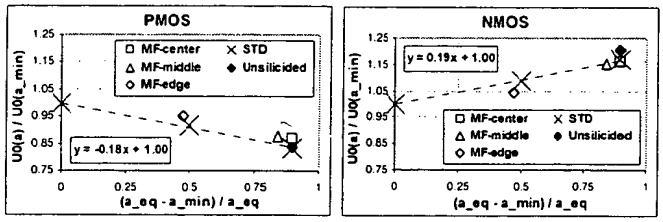

Figure 13. Mobility measurements on Unsilicided and Multi-Finger shape MOSFETs (see Figure 12) compared to standard shape ones (STD) and U0(a_{eq}) model. Both Unsilicided and Multi-Finger MOSFET mobility variations fairly match STD shape ones (with cobalt silicide) and U0(a_{eq}) model. Thus, stress effects of $CoSi_2$ formation process can be neglected.

To compare the importance of present-day $CoSi_2$ processes stress, versus STI induced one, an unsilicided version of the standard shape MOSFETs has been tested. Indeed, to check whether distance to STI "a_{eq}" or "Drain/Source" size is the relevant dimensional parameter for stress modeling, individual gate fingers in an equally spaced Multi-Finger structure with $CoSi_2$ (see Figure 12) have been tested too.

Identical mobility variations are observed on Unsilicided and on STD shape (with $CoSi_2$) MOSFETs (see Figure 13) and each finger of the Multi-Finger structure closely match STD shape MOSFETs and U0(aeq) model. Consequently, the stress effects of the used $CoSi_2$ formation process can be neglected.

SPICE Models Correction and Applications

BSIM3 simulation models, calibrated on "a_{min}-MOSFETs", have been modified adding (2) to account for mobility variations according to MOSFET geometry (see Figure 14 and Figure 15). Algorithms for "a_{eq}" computing have been added to Layout Extractor Tools, in 0.12µm and 0.18µm Design Kits (DK), in order to generate Spice-like circuit net lists including "a_{eq}" data.

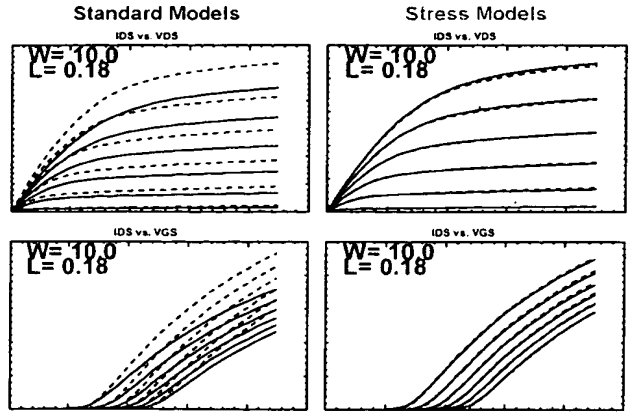

Figure 14. PMOS transistor stress modeling for a=10um: measurements (solid lines) versus simulations (dashed lines). Stress effects account leads to an accurate model.

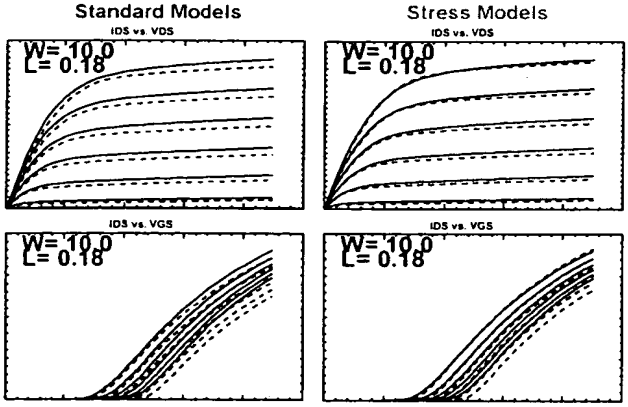

Figure 15. NMOS transistor stress modeling for a=10um: measurements (solid lines) versus simulations (dashed lines). Simulation model accuracy is significantly improved by stress effects account.

The modified DK has been used to optimize a special I/O circuit in 0.18µm CMOS technology (see Figure 16). In this I/O circuit version major functional characteristics rely on the "$U0_{NMOS}/U0_{PMOS}$ ratio" of output stage MOSFETs, presenting "a_{eq} >>10µm" (i.e. maximum U0 discrepancy with respect to standard simulation models). $U0_{NMOS}$ and $U0_{PMOS}$ discrepancy contribution to "$U0_{NMOS}/U0_{PMOS}$ ratio" are additive, leading to up to 30% simulation error.

The circuit has been fabricated and tested showing proper functionality. Simulation results of the fully functional I/O circuit, using the standard and our novel simulation model, are shown in Figure 17. The latter allows proper simulation, closely matching circuit measurements. The former predicts an overestimated Crossing Point and a wrong T_{RISE}/T_{FALL} ratio.

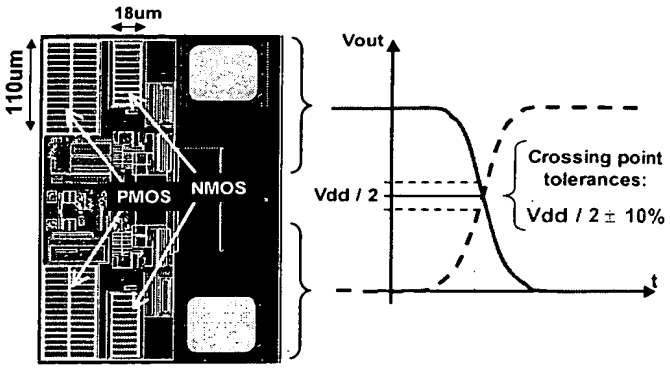

Figure 16. I/O Circuit and Crossing Point tolerances. Differential output signals Crossing Point and "T_{RISE} / T_{FALL} ratio" relies on "$U0_{NMOS}/U0_{PMOS}$ ratio" of output stage MOSFETs, presenting "a_{eq}>>10µm" (shunt multi-finger MOSFETs sharing a huge Active Area).

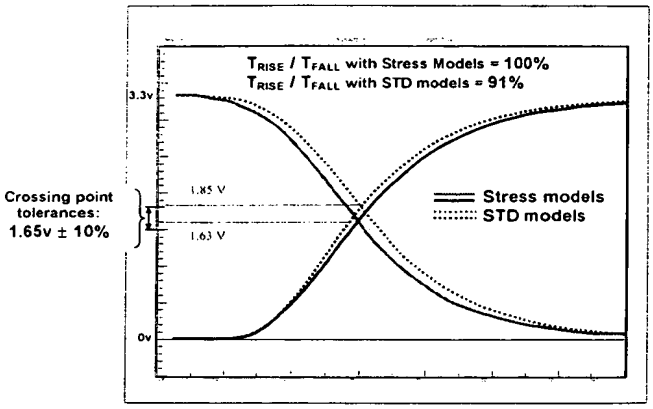

Figure 17. Fully functional I/O Circuit simulated with Standard Models (STD) and Stress Models. The latter allows proper simulation, which predictions closely match circuit measurements. The former predicts an overestimated Crossing Point and a wrong T_{RISE} / T_{FALL} ratio.

Conclusions

The excellent agreement between mechanical simulations, modeling and electrical results confirms that STI induced mechanical stress is the dominant mechanism for stress variation in the channel, resulting in carriers mobility modulation as a function of MOSFET geometry.

The presented mobility model proved to be an efficient way to modify standard MOSFET simulation models, so that STI induced mechanical stress effects can be taken into account in IC design. This early validation allows to extend its use to the 90nm node and below.

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Reduction of STI/active Stress on 0.18µm SOI Devices Through Modification of STI Process

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Advanced Micro Devices, Sunnyvale, CA USA

Abstract:

Stress from shallow trench isolation was found to cause up to 19% variation in 0.18µm technology SOI devices. Partially depleted SOI devices were fabricated on a 0.18µm technology with 100nm thick silicon film and 200nm thick buried oxide. The STI edge parallel to the edge of the gate was found to induce compressive stress on the SOI device. For N-Ch devices, closer proximity of the STI edge resulted in a 18% degradation of the long channel transconductance (gm,max). The opposite trend was observed for P-Ch devices. STI stress reduction was achieved by switching the liner oxidation step in the STI formation from before the trench oxide fill to after. The STI stress improvement resulted in 50% reduction of the dependence of the long channel gm,max to the proximity of the STI trench edge. The lower STI stress improved the device variation between different SOI transistor layout geometries.

Introduction:

Stress impact on carrier mobility is an important issue for deep-submicron high-performance CMOS transistors. Since devices in thin SOI film could be subjected to a significantly higher stress than bulk devices, it is crucial to minimize stress effect in SOI technology. A change in carrier mobility caused by stress from different isolation processes has been recently reported both for shallow trench isolation (STI) on bulk transistors [1] and for LOCOS isolation on SOI transistors [2]. This paper investigates the effect of STI-induced stress on device performance in thin film SOI technology. Gm,max is used to monitor the effect of the stress since it varies linearly with mobility. A modified STI formation process is shown to be effective to reduce the stress effect.

Experiment:

Test transistors with different active size were used to measure the effect of STI stress on the device characteristics. Two sizes were used, one with the active edge spaced 0.36µm away from the side of the transistor (near STI edge device) and another spaced 7µm away (far STI edge device), as shown in Figure 1. The large spacing prevents any influence of the STI stress from affecting the transistor, while the small spacing maximizes the effect. Comparing the long channel gm,max of the transistors can monitor the effect of the STI stress on carrier mobility. Figure 2 shows a cumulative probability plot of the gm,max for both the near and far STI edge devices for a set of wafers. For the N-Ch devices the STI stress causes a 18% degradation of gm,max, and for the P-Ch devices a 19% improvement. This result is consistent with the influence of compressive stress from the STI [2].

The STI formation process can induce compressive stress due to the liner oxide formation. Typical STI formation requires to growth of a thermal oxide liner to act as high quality interface between the oxide fill and the device. The thermal oxidation process has enhanced oxidation at the silicon film to buried oxide interface as shown in Figure 3. This enhanced oxidation causes an uplifting of the silicon film, resulting in compressive stress in the channel region.

The influence of the liner oxide formation on the STI stress can be reduced by switching the liner oxide formation step from before the trench oxide fill to after. By filling the trench with oxide prior to the thermal oxidation step, the oxidation process is reduced at the silicon/buried oxide interface. This reduces the uplifting of the silicon film and the amount of stress.

A set of wafers was processed with the liner oxidation after the trench fill and the long-channel gm,max measured for both the near and far STI edge transistors. As shown in Figure 4, the difference between the near and far STI edge transistor gm,max is significantly reduced for the post trench fill liner oxidation wafers as compared to the pre trench fill liner oxidation wafers shown earlier. The post trench fill liner oxidation wafers show 50% reduction for N-Ch and 48% reduction for P-Ch . This reduction indicates that the post trench fill liner process has significantly less STI stress than the pre trench fill liner process.

The use of the post trench fill liner oxide results in a significant reduction in the variation in the long channel gm,max with active area. This reduction can reduce the variability between individual devices and stacked gate devices in a circuit layout. The individual devices would be comparable to the near STI edge transistors, while the stacked gate devices would be comparable to the far STI edge transistors.

Conclusion:

Stress was monitored in 0.18µm SOI devices through the long channel gm,max. 18-19% variation in the long channel gm,max was observed between devices with near STI edges as compared to devices with far STI edge. The variation was reduced by ~50% when the STI stress was reduced, by switching the liner oxide from before the trench oxide fill to after the trench oxide fill. Reduction of STI stress improves the variability of the SOI devices due to layout geometry differences.

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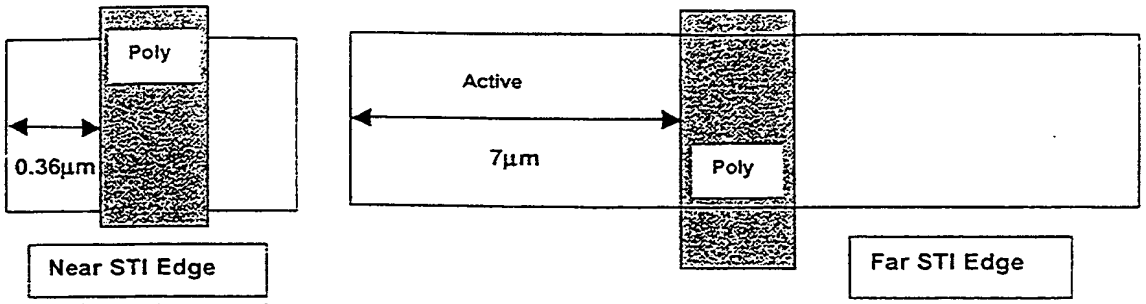

Figure 1: Schematic drawing of the dimensions of the different active sized transistors. The near STI edge devices have the STI edge 0.36µm away from the gate edge. The far STI edge devices have the STI edge 7µm away from the gate edge.

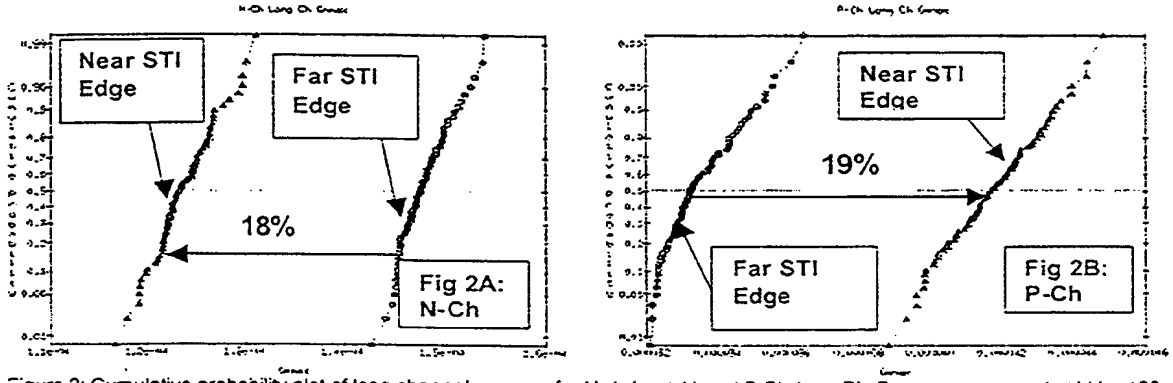

Figure 2: Cumulative probability plot of long channel gm,max for N-ch (part A) and P-Ch (part B). Gm,max measured at Vd = 100mV (W/L= 10µm/2.7µm). N-Ch shows a 18% degradation in the nominal gm,max from far STI edge (low stress) to near STI edge (high stress). P-Ch shows a 19% improvement in the nominal gm,max from far STI edge (low stress) to near STI edge (high stress). This coorelates to compressive stress on the silicon.

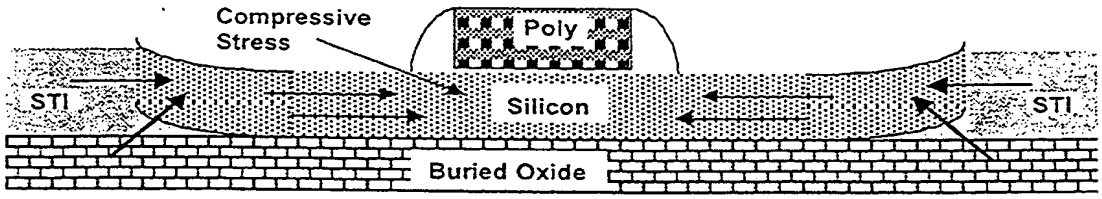

Figure 3: Schematic of cross-section of SOI transistor showing the encroachment of the STI at the silicon/ buried oxide interface due to the thermal liner oxidation process prior to the trench oxide fill. This causes the silicon film to be lifted at the STI boundary resulting in compressive stress in the channel. Arrows show direction of stress.

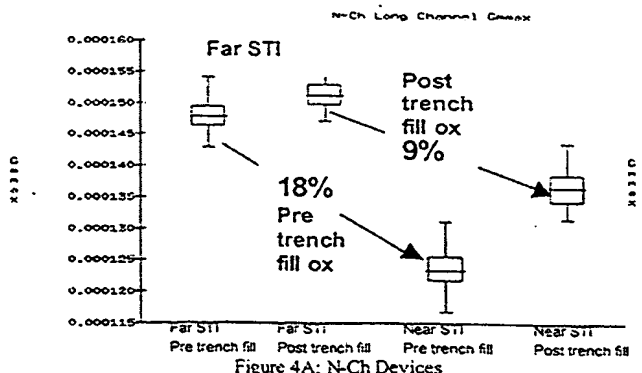

Figure 4A: N-Ch Devices

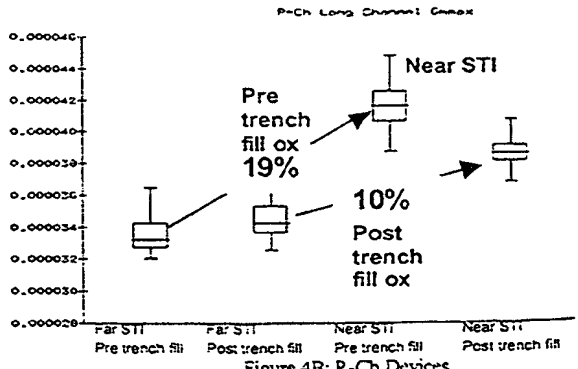

Figure 4B: P-Ch Devices

Figure 4: Box plots of long channel gm,max for N-Ch (4A) and P-Ch (4B) comparing pre trench fill liner oxidation with post trench fill liner oxidation. N-Ch shows ~50% reduction in the long channel gm,max variation with the post trench fill liner oxidation. P-Ch shows a comparable ~48% reduction with the post trench fill liner oxidation. Arrows indicate shift from far STI edge device to near STI edge device.

[10]

Stress Induced Defects and Transistor Leakage for Shallow Trench Isolated SOI

Jeffrey W. Sleight, *Member, IEEE*, Chuan Lin, and Gregory J. Grula, *Member, IEEE*

***Abstract*—Anomalous leakage currents are observed for shallow trench isolated SOI transistors. The leakage effect is caused by stress induced dislocations in the device silicon islands. These dislocations are observed using cross-sectional TEM analysis. For the shallow trench isolation process employed, the leakage is most pronounced on SIMOX wafers when the buried oxide thickness is scaled down to 100 nm. Limiting fabrication stresses to a minimum is critical for eliminating this leakage defect and in obtaining a robust, high yielding SOI STI process.**

I. Introduction

RECENT work has shown that the type of CMOS device isolation technology employed (i.e., LOCOS or STI) in defining silicon on insulator (SOI) transistors can have a profound impact upon both the device mobility [1], [2] and defectivity [3]. The underlying cause in both cases is the stress that the devices undergo during the isolation process and the stress that remains after the processing is completed. Recent work by Iwamatsu *et al.* [4] observes anomalous source to drain leakage in their short-channel mesa isolated SOI devices due to the diffusion of the source and drain dopant along the device edges. In our work, we will examine a defect induced leakage effect for shallow trench isolated (STI) SOI devices. While this effect possesses electrical signatures similar to the mesa isolated case, the physical origin responsible for the leakage is very different and is similar to STI related defects observed in conventional bulk CMOS [5].

II. Process

For the results we present in this paper, low dose SIMOX SOI wafers with an initial silicon thickness of 170 nm and a buried oxide thickness of 100 nm are used. During processing, approximately 20 nm of silicon is consumed for a final silicon thickness of 150 nm. Shallow trench isolation (STI) is employed for device isolation. A sidewall oxidation of modest thickness is performed and the trenches are filled with SiO_2. Channel stop implants were performed and the source/drain dopants were boron and arsenic, which received a post-implant RTA. The gate oxide thickness is 6 nm and the nominal on-wafer poly-silicon gate length is 0.32 μm. The partially depleted SOI MOSFET's have moderately doped source/drain extensions, oxide/nitride spacers, N^+/P^+ doped poly-silicon gates, and cobalt silicide on the source/drain and gate regions. Further process technology details are given elsewhere [6].

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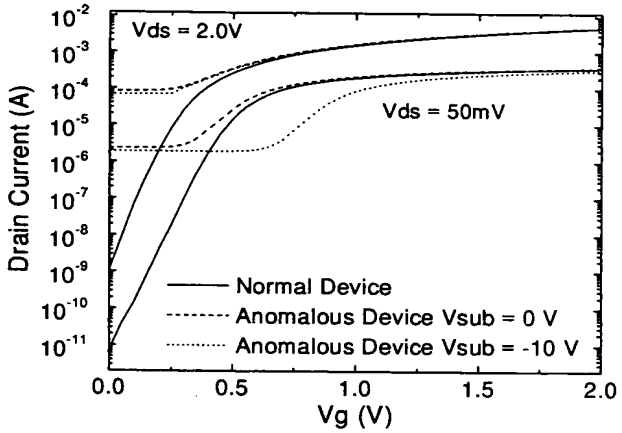

Fig. 1. I_d–V_g characteristics of a normal device (solid) and a device with anomalous source to drain leakage under a substrate bias of 0 V (dash) and −10 V (dot). Device width/length is 14/0.35 μm.

III. Device Electrical Behavior

Fig. 1 shows I_d–V_g behavior for a normal n-MOSFET as well as for a MOSFET that shows the anomalous leakage at low gate bias. The anomalous device is shown with both a substrate bias of 0 and −10 V. Unlike edge leakage in SOI STI MOSFET's, which typically causes a shoulder in the I_d–V_g due to parasitic edge transistors, the observed leakage value shows little dependence upon applied substrate bias. For edge leakage, substrate bias will usually completely suppress such leakage [7]. Fig. 2 shows that for the condition where $V_g = 0$ V, the resistance of the leakage is constant. Both the independence of the leakage current on V_g and the linear resistance with V_{ds}, are not consistent with leakage through a parasitic edge device.

As noted in the earlier study of mesa isolated devices [4], we also observe that the leakage defect only occurs on shorter channel length devices. Fig. 3 shows the probability of the defect versus channel length. The leakage is only observed in device lengths at or below 1.4 μm and the frequency tends to increase as the channel length (and width) decreases. Differing from the mesa isolated case, we do observe the leakage for H-type gate transistors (transistors which are gate isolated on the edges, so there is no exposed source/drain edge) with

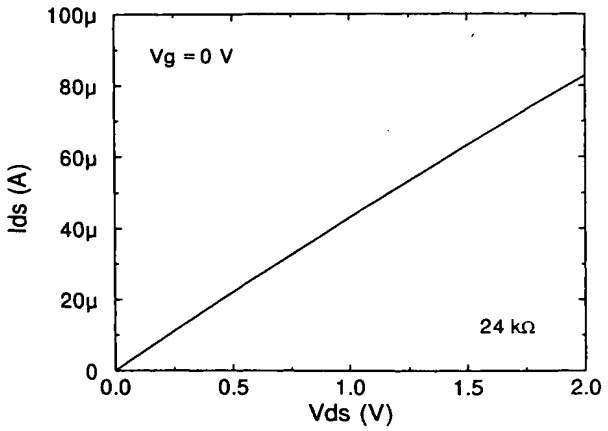

Fig. 2. Drain current versus voltage for a device showing the anomalous leakage (W/L = 14/0.35 μm).

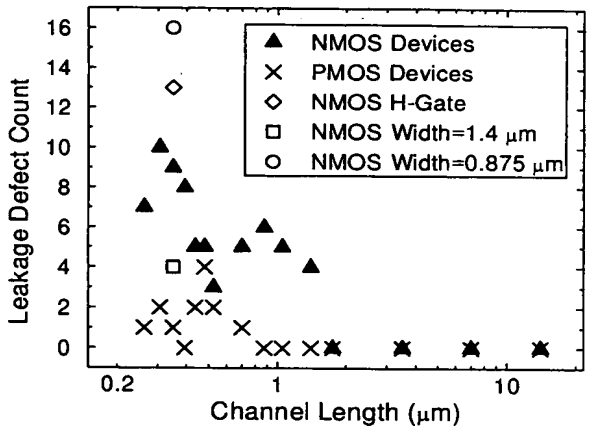

Fig. 3. Probability of the leakage defect versus device channel length. The device widths are 14 μm except where noted. A total of 156 sites over three wafers were measured for each device shown.

about the same frequency as with the normal transistors. The H-gate transistors are designed with a 0.35-μm wide body tie connection to the channel, which should ensure that they interact similarly with the processing as other non-H-gate devices of the same device width and length. This observation rules out that the leakage is due to source/drain dopant diffusion along the device edge, which was the mechanism observed in the mesa isolation case [4].

IV. Material Analysis

Fig. 4 shows a TEM cross section of a device through the width direction, under the gate poly region. In the active device silicon island region, two smaller (left) and one larger (right) dislocation defects are clearly visible. The gate length in this device is 0.35 μm. These dislocation defects are similar to those observed to cause leakage in bulk silicon CMOS STI transistors [5]. Similar defects were observed in many other short-channel devices. We therefore propose that these dislocation defects are also responsible for the anomalous leakage observed on the SOI STI transistors. For

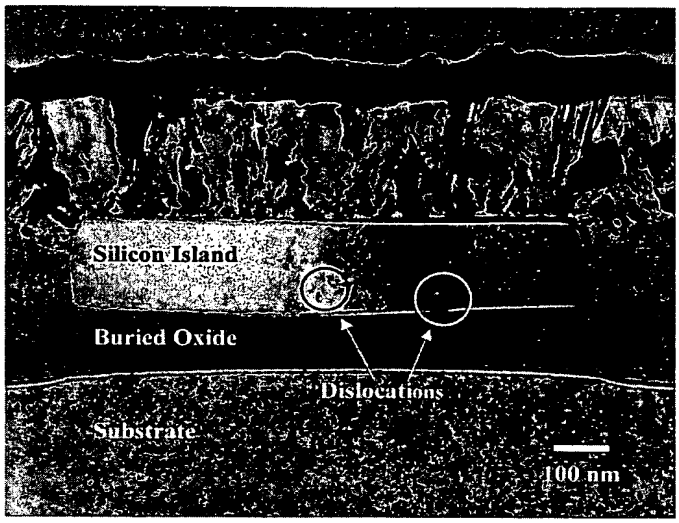

Fig. 4. Cross-sectional TEM of the active silicon island between source and drain (under poly) showing the dislocation defects (W/L = 0.875/0.35 μm).

the defect to become electrically active, it must be doped by the source/drain dopant, as well as span the entire distance from the source to the drain of the device. Both of these requirements would explain the tendency to observe the defect only at the shorter channel lengths. The lower occurrence of the defect for PMOS devices indicates that the PMOS source/drain dopant (B) may be less effective than the NMOS source/drain dopant (As) in doping the dislocation defect.

An important difference between our results on SOI and the results on bulk CMOS is that the SOI results are a strong function of the starting material type. For example, SIMOX wafers from a different vendor with thicker buried oxides (both 200 and 350 nm), fabricated in the exact same isolation process do not exhibit any anomalous leakage. Note that this result is consistent with studies that show that stresses are greater for SOI devices formed on thinner buried oxides [3]. This highlights the important point for SOI STI which is that stress created during the isolation process must be minimized as much as possible. Additionally, fabrication imposed stress has a greater impact as the SOI material is scaled to thinner buried oxide values. Furthermore, the initial stress in the SOI wafer prior to any isolation processing may also play a role independent of the thickness of the buried oxide. This was evident in similar leakage problems that occurred in BESOI material with thicker buried oxide layers (comparable to medium dose SIMOX). The higher occurrence of this defect at narrower device widths is also consistent with the role that stress plays in the defect generation, as the stresses are generally higher for smaller width silicon islands.

V. Conclusions

We observe anomalous leakage for shallow trench isolated SOI transistors with a thin (100 nm) buried oxide layer thickness. The leakage is attributed to dislocation defects that occur in the silicon island, due to the stress that the silicon island undergoes during the isolation process. Limiting

fabrication stresses to a minimum is critical for eliminating this leakage defect and in obtaining a robust, high yielding SOI STI process.

ACKNOWLEDGMENT

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Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices

Daewon Ha, Changhyun Cho, Dongwon Shin, Gwan-Hyeob Koh, Tae-Young Chung, and Kinam Kim

Abstract—**As the density of dynamic random access memory (DRAM) increases up to giga-bit regime, one of the important problems is the control of the process-induced defects and damage. Although the shallow trench isolation (STI) is widely used for deep submicron devices, it has a great possibility of generating STI dislocations due to its inherently large mechanical stress and damage. When STI dislocations are located within the depletion region of pn junction, anomalous junction leakage current could flow. This junction leakage current degrades the memory cell data retention time and the standby current of DRAM. We resolved the problems from STI dislocations as follows; the crystal defects and the mechanical stress were reduced by optimizing the implantation condition and the densification temperature of trench filled high-density plasma (HDP) oxide, respectively. In addition, the residual mechanical stress before source/drain implantation was relieved through rapid thermal nitridation (RTN). By using these methods, STI dislocations were successfully clamped outside the depletion region of pn junction.**

Index Terms—**Data retention time, dislocations, dynamic random access memory (DRAM), junction leakage current, shallow trench isolation (STI).**

I. Introduction

DYNAMIC random access memory (DRAM) devices have been developed in pursuit of the high-memory density capability and the reliable performance with the continuous shrinkage of the minimum feature size. As the memory density increases up to giga-bit regime, several challenges should be encountered and controlled very carefully: the increase of standby current due to a large chip size and the decrease of memory cell data retention time due to a small memory cell capacitor area [1]. In subquarter micron technology, shallow trench isolation (STI) has been the most predominant isolation method for many reasons that the abrupt transition of active/field region, the good planar surface, the reduced junction capacitance and the improved data sensing margin [3], [4]. Inherently large mechanical stress and damage in STI, nevertheless, combined with the subsequent process-induced stress and defects, would generate STI dislocations. In recent studies, abnormally large leakage current through junction and/or transistor was attributed to the presence of STI dislocations within the junction depletion region. Ikeda *et al.* [6] showed that the mechanical stress from device structure and source/drain annealing could generate dislocations even though LOCOS isolation method was adopted. They proposed the two step annealing for both the activation of source/drain dopant and the minimization of the mechanical stress. Ishimaru *et al.* [7] and Park *et al.* [8] proposed the technology of diminishing the residual stress in STI through the high-temperature densification and the optimized combination of trench filling TEOS-O_3 oxide, respectively. Damiano *et al.* [9] showed that the crystal defects from source/drain implantation would generate STI dislocations during the following high-temperature thermal annealing and the reduced mechanical stress alone could not thoroughly eliminate the STI dislocations. By applying an additional oxidation process after source/drain implantation, they could obtain the dislocations-free STI. In our experiment, however, the short-channel effect of PMOS transistor was significantly aggravated due to the oxidation enhanced boron diffusion.

In this paper, the behavior of STI dislocations and the effect on the pn junction characteristics during the fabrication of an experimental 16-Mb DRAM with the minimum feature size of 0.15 μm will be described in Section II. In Section III, the memory cell data retention time imposed by the anomalous junction leakage current and the technology of clamping STI dislocations outside the depletion region of pn junction without the degradation of device performance through the rapid thermal nitridation (RTN) instead of the gate reoxidation and the careful control of mechanical stress in STI and process-induced defects are discussed. Finally, conclusions are followed in Section IV.

II. Behavior of STI Dislocations

There are several factors to generate STI dislocations; crystal defects, mechanical stress and thermal annealing. During the fabrication of DRAM devices, they are reacted with other in a complex manner. Therefore, it is very helpful to investigate each factor and its role of generating STI dislocations. Crystal defects are primarily resulted from ion implantation. Although ion implantation has been indispensable by virtue of the precise control of doping concentration and profile, it induces crystal defects and needs thermal annealing for dopant activation. Several ion implantation steps are essentially adopted for fabricating DRAM devices; well, punchthrough stop, threshold voltage adjust, source/drain, and contact hole formation. Among these steps, source/drain and contact hole implantation mainly provide the seeds of STI

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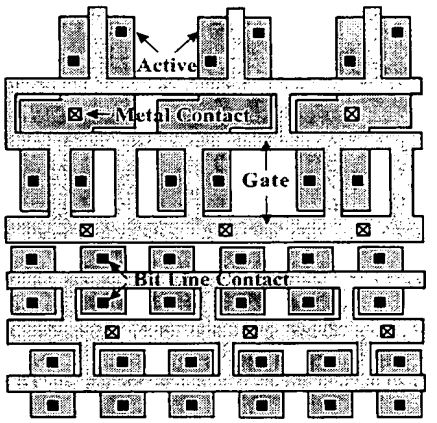
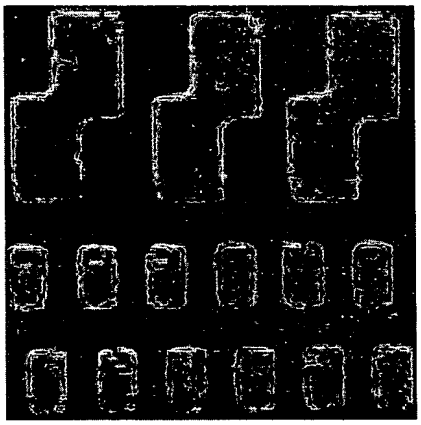
dislocations because low dose ($\leq 1 \times 10^{14}$ cm^{-2}) implantation induces a little crystal defects regardless of the dopant species [10]. In DRAM fabrication, a few thermal annealing (or oxidation) steps are necessitated for the interlayer dielectric densification and the capacitor formation. During the thermal annealing, crystal defects from ion implantation generate STI dislocation, which moves along the mechanical stress in STI and interacts with others to evolve a larger dislocation [11].

An experimental 16-Mb DRAM with the capacitor-over-bit line (COB) structure was manufactured using 0.15-μm technology node and the fabrication sequence was reported in our previous study [2]. Fig. 1 shows (a) the layout of a sense amplifier (S/A) region and the plan-view SEM images of a S/A region after strip off and wright etching (b) before and (c) after capacitor formation, respectively. Because most of the thermal annealing after source/drain implantation is accomplished during the capacitor formation, STI dislocations were investigated before and after capacitor formation. In order to observe the STI dislocations, the samples were etched using diluted HF solution and immersed in wright solution. Most of STI dislocations, confined inside the contact hole before the capacitor formation [Fig. 1(b)], have moved toward the STI corner and the STI boundary beneath the gate after heat treatment of Ta_2O_5 capacitor dielectric materials [Fig. 1(c)]. The driving force and direction of STI dislocations were generated by the thermal energy during capacitor formation and the mechanical stress in STI, respectively. Fig. 2 shows the stress simulation result of STI using TSUPREM. The maximum stress exists at the trench corner, which is coincident with previous studies [15], [16].

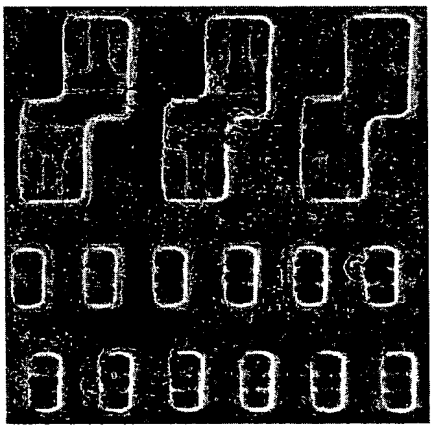
Fig. 3(a) shows the cross-sectional TEM image of STI dislocations. As long as STI dislocations are located outside the depletion region of junction, they could not have any detrimental effect on the pn junction characteristics. When STI dislocations penetrated the depletion region, however, they acts as the recombination/generation center between the band gap and the abnormally large leakage current of reverse-biased junction could flows through them [12]. Fig. 3(b) shows the reverse-biased leakage current of p^+n junction in an actual sense amplifier (S/A) before (filled triangle) and after (filled circle) capacitor formation. Even though a small reverse bias (<3.0 V) is applied, anomalously large junction leakage current flows especially for the case of after the capacitor formation. This result implies that the thermal annealing for capacitor formation collects the crystal defects and makes them grow vertically enough to penetrate the depletion region.



(a)



(b)



(c)

Fig. 1. (a) Layout of a sense amplifer (S/A) region and the plan-view SEM images of a S/A region after strip off and wright etching (b) before and (c) after capacitor formation, respectively.

III. Impact of STI Dislocations on DRAM Performance

The memory cell data retention time can be decreased by the large leakage current through cell transistor and storage node junction. In order to suppress the sub-threshold leakage current of cell transistor, the threshold voltage is usually adjusted around 1.0 V regardless of the DRAM density. Therefore, the substrate doping concentration should be increased with the shrinkage of the minimum feature size. Because of the increased substrate doping concentration, junction leakage current should be carefully controlled especially for the high-density DRAM [1]. The effect of junction leakage current on the memory cell data retention time can be evaluated as below.

When the cell storage capacitor has a high data (V_{CC}) and the bit lines are precharged with 0.5 V_{CC}, the total charge ($Q_{T,I}$) becomes

$$Q_{T,I} = C_S \times (V_{CC} - \Delta V_L) + C_{BL} \times \tfrac{1}{2} V_{CC} \qquad (1)$$

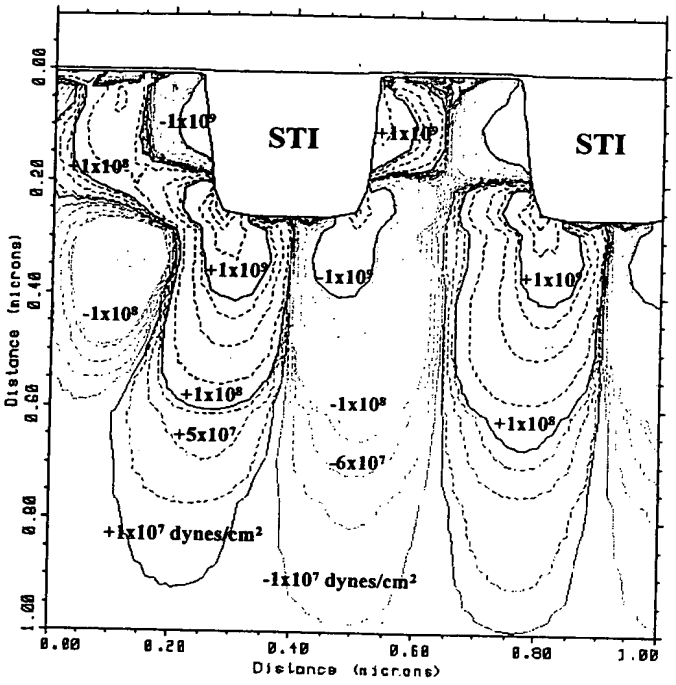


Fig. 2. Stress simulation result of STI using TSUPREM. The maximum stress exists at the trench corner.

where C_S and C_{BL} are the cell storage capacitance and the parasitic bit-line capacitance, respectively. V_{CC} is the operation voltage and ΔV_L is the data loss at the storage node due to the leakage current through junction, transistor, and capacitor.

When the memory cell is selected, the data stored in the cell storage capacitor is transferred to bit-line and the total charge ($Q_{T,F}$) becomes

$$Q_{T,F} = (C_S + C_{BL}) \times V_{BL}. \tag{2}$$

According to the charge conservation law, the total charge before charge transfer ($Q_{T,I}$) should be equal to that after charge transfer ($Q_{T,F}$). Therefore, we can obtain the bit line voltage (V_{BL}) as follows:

$$V_{BL} = \frac{C_S}{C_S + C_{BL}} \times (V_{CC} - \Delta V_L) + \frac{C_{BL}}{C_S + C_{BL}} \times \tfrac{1}{2} V_{CC}. \tag{3}$$

Since the complementary bit line is precharged with 0.5 V_{CC}, the differential voltage between two bit line (ΔV_{BL}) becomes

$$\Delta V_{BL} = V_{BL} - V_{\overline{BL}} = \frac{C_S}{C_S + C_{BL}} \times \left(\tfrac{1}{2} V_{CC} - \Delta V_L\right). \tag{4}$$

The data loss at storage node can be defined as

$$\frac{C_S \times \Delta V_L}{T_{RET}} = I_{LEAK} \tag{5}$$

where T_{RET} is the memory cell data retention time and I_{LEAK} is the total leakage current at the storage node. Using (4) and (5), the relationship of the memory cell data retention time and the leakage current at storage node can be obtained as follows:

$$T_{RET} = \frac{C_S \times \frac{1}{2} V_{CC} - \Delta V_{BL} \times (C_S + C_{BL})}{I_{LEAK}}. \tag{6}$$

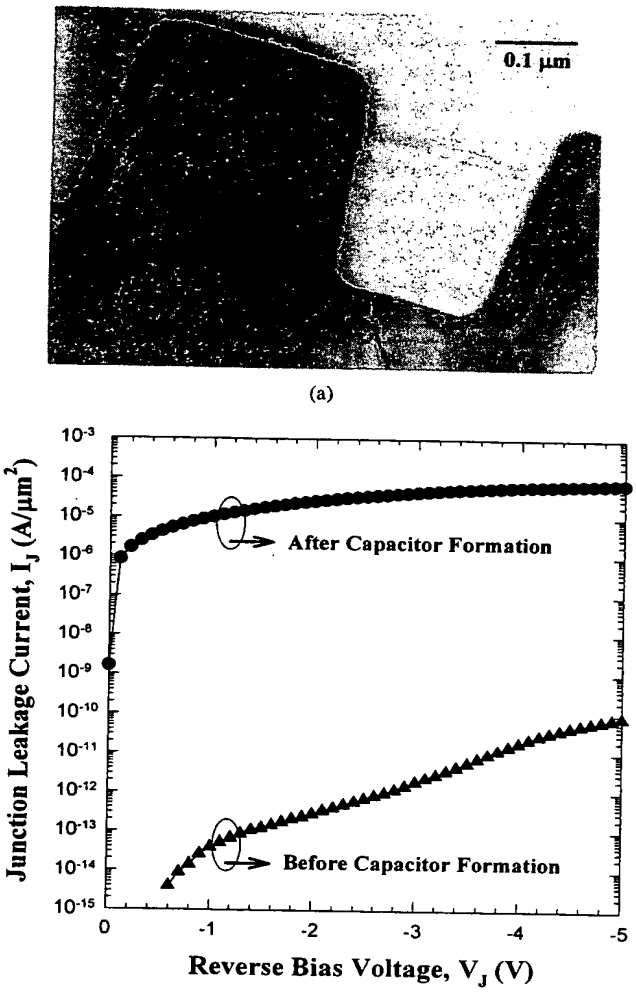


Fig. 3. (a) Cross-sectional TEM image of STI dislocations and (b) the reverse-biased leakage current before (filled triangle) and after (filled circle) capacitor formation measuring p^+n junction in an actual sense amplifier (S/A).

Fig. 4 shows the memory cell data retention time versus the leakage current at storage node with the operation voltage as a parameter. The cell storage capacitance (C_S), the parasitic bit line capacitance (C_{BL}), and the bit line sensing voltage (ΔV_{BL}) are assumed to be 25 fF, 130 fF, and 80 mV, respectively. When the leakage current at storage node is higher than 5×10^{-13} A/cell, the memory cell data retention time is considerably decreased for low voltage operation. Because the data retention time of DRAM devices is determined by weak memory cells, the refresh characteristics could be significantly aggravated by memory cells which suffer from the anomalously large junction leakage current induced by STI dislocations.

In order to eliminate STI dislocations, many efforts were concentrated on minimizing the mechanical stress in STI and the crystal defects from ion implantation. According to Ishimaru *et al.* [7], the densification of TEOS-O_3 oxide at high temperature (1200 °C) minimizes the oxide etch-rate in HF solution and the residual stress in STI at the same time, but this may induce other problems such as wafer

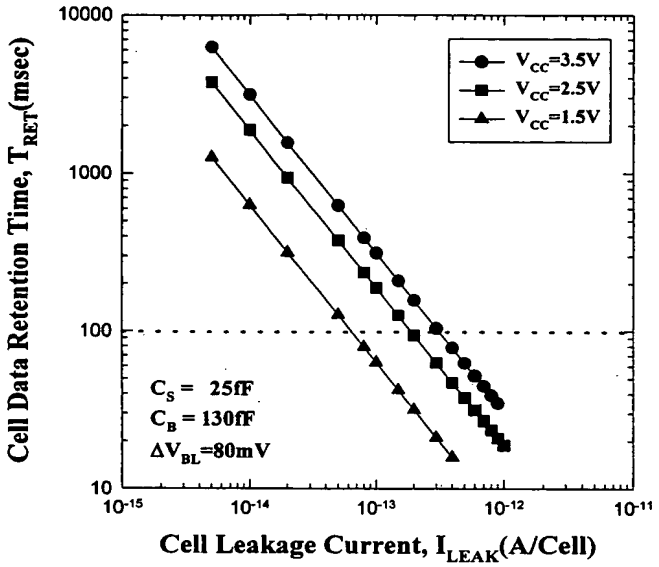


Fig. 4. Memory cell data retention time versus the leakage current at storage node with the operation voltage as a parameter.

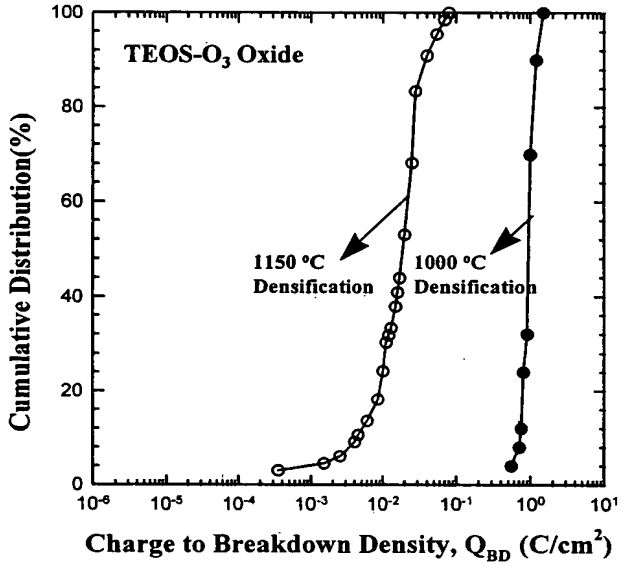
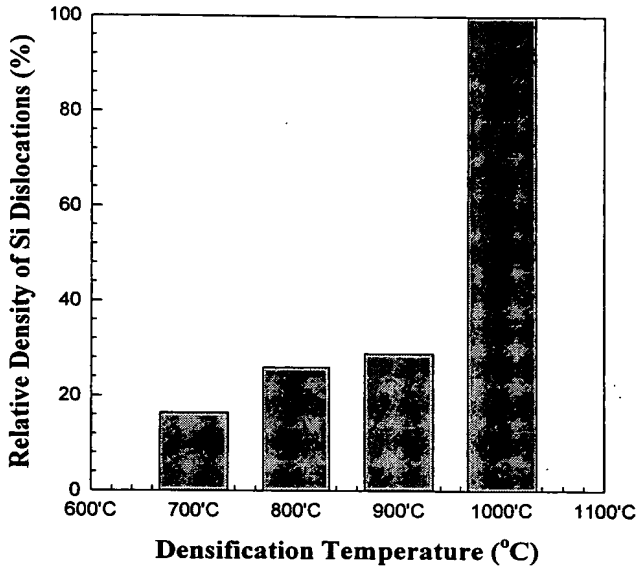
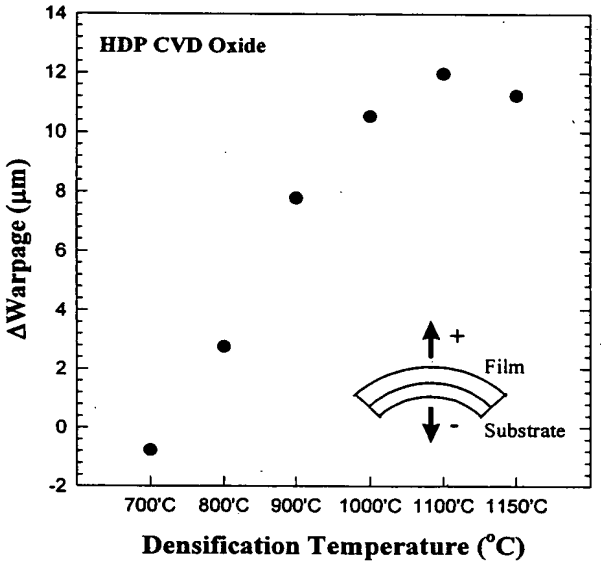


Fig. 5. Result of charge to breakdown density (Q_{BD}) measurement for different densification temperature of TEOS-O_3 oxide.



(a)



(b)

Fig. 6. (a) Normalized density of STI dislocations and (b) the wafer warpage for various densification temperatures of trench filling high-density plasma (HDP) oxide.

warpage and gate oxide degradation. Fig. 5 shows the result of charge-to-breakdown density (Q_{BD}) measurement for different densification temperature of TEOS-O_3 oxide using STI edge intensive test pattern. The gate oxide reliability was severely degraded for the high-temperature densification of TEOS-O_3 oxide. This result indicates that the gate oxide at the STI edge was degraded due to the stress, which was induced from the large volume shrinkage of TEOS-O_3 oxide at high-temperature densification. High-density plasma (HDP) oxide has advantages of the superior step coverage and the low etch-rate in HF solution even though the densification is applied at relatively low temperature [5]. In our experiment, the trench was filled with HDP oxide, followed by densification at the temperature ranging from 700 to 1000 °C. Fig. 6 shows the normalized density of STI dislocations and the wafer warpage for various densification temperatures of HDP oxide. The less STI dislocations were observed as the lower densification temperature was applied by virtue of the reduced mechanical stress [14].

It has been known that the crystal defects are strongly dependent on the implantation conditions (e.g., dopant species and dose) [10]. The different doses of arsenic and phosphorus were investigated for n^+ contact hole implantation. Fig. 7 shows the normalized density of STI dislocations for different implantation conditions. STI dislocations are decreased about 80% by implanting arsenic (2×10^{15} cm^{-2}) compared to

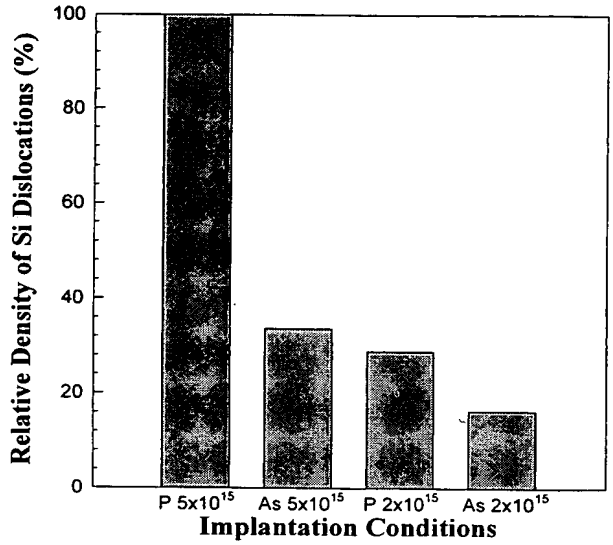


Fig. 7. Normalized density of STI dislocations for different implantation conditions.

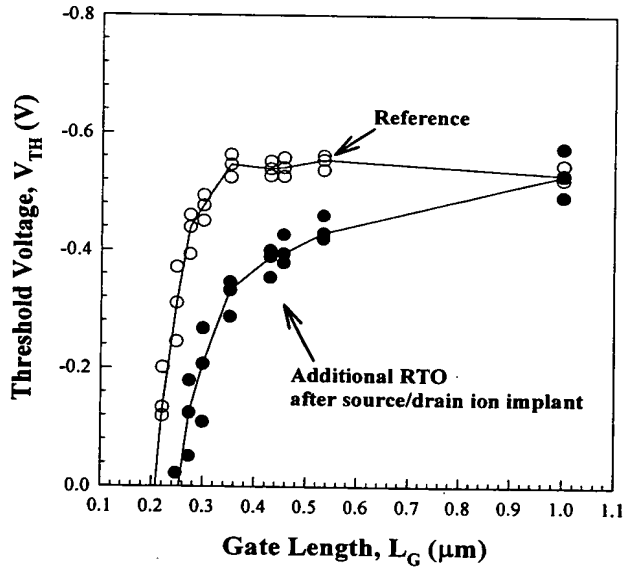
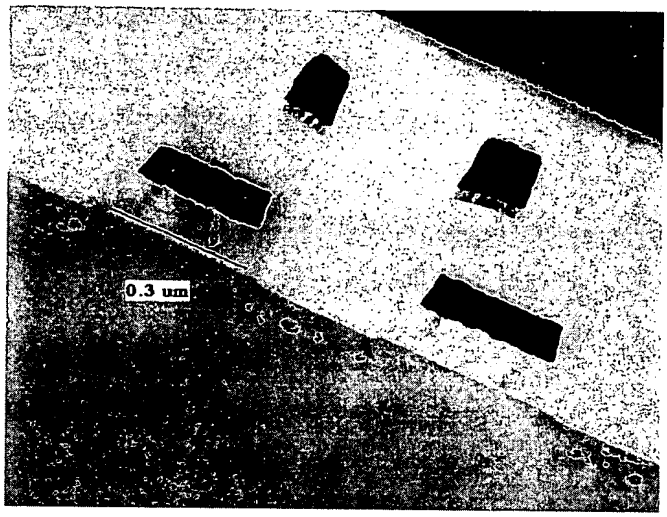


Fig. 8. Threshold voltage (V_{TH}) roll-off characteristics of buried channel PMOS. When the rapid thermal oxidation (RTO) was additionally adopted after source/drain implantation (filled circle), the short-channel effect of buried channel PMOS is significantly aggravated below 0.35 μm channel length due to the oxidation-enhanced boron diffusion.

phosphorus (5×10^{15} cm^{-2}). This result implies that the implantation of relatively higher dose and lighter ion produces more crystal defects which generate STI dislocations.

For the purpose of reducing the overall crystal defects before capacitor formation, it is necessary to cure the crystal defects from source/drain implantation. The rapid thermal oxidation (RTO) was additionally applied after source/drain implantation. STI dislocations were fully eliminated by the gettering effect of oxidation and no degradation of the junction characteristics was observed. However, the short-channel effect of buried channel PMOS was severely aggravated



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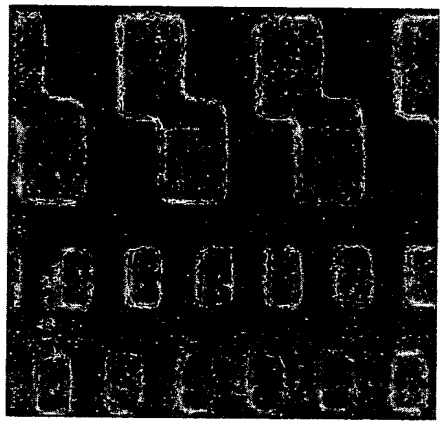


(b)

Fig. 9. (a) Cross-sectional TEM and (b) the plan-view SEM images of STI dislocations when rapid thermal nitridation (RTN) was performed instead of gate reoxidation.

below 0.35 μm channel length due to the oxidation-enhanced boron diffusion, as depicted in Fig. 8. This result implies that the doping profiles of channel and source/drain of buried channel PMOS were indispensably redistributed during the additional RTO. In previous report [13], the activation energy of eliminating STI dislocations (5.0 eV) is larger than that of boron diffusion (3.46 eV). For high-density DRAM devices, therefore, it is not adequate to apply the heat treatment additionally after source/drain implantation for eliminating STI dislocations without the redistribution of boron.

As long as STI dislocations are located outside the depletion region, they could not have any detrimental effect on the pn junction characteristics. Therefore, STI dislocations are tried to be pinned at their generation site by relieving the cumulated mechanical stress before reacting with the crystal defects from source/drain implantation. The mechanical stress is induced during the gate formation; gate oxidation, gate poly doping ($POCl_3$), and so on. In order to relieve the cumulated mechanical stress before source/drain implantation,

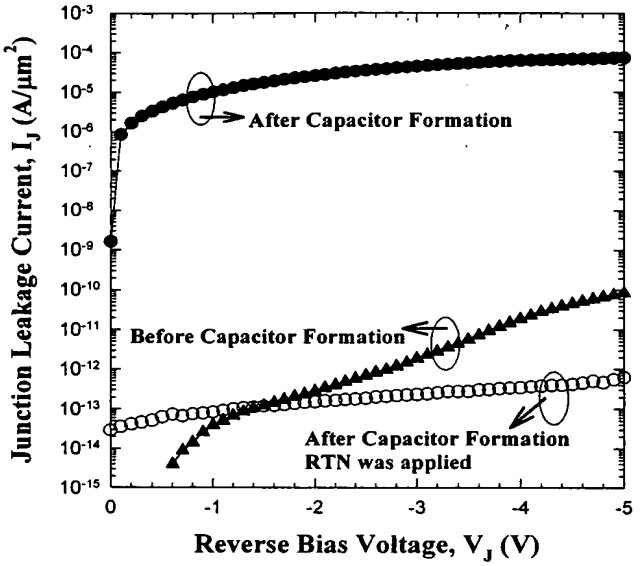
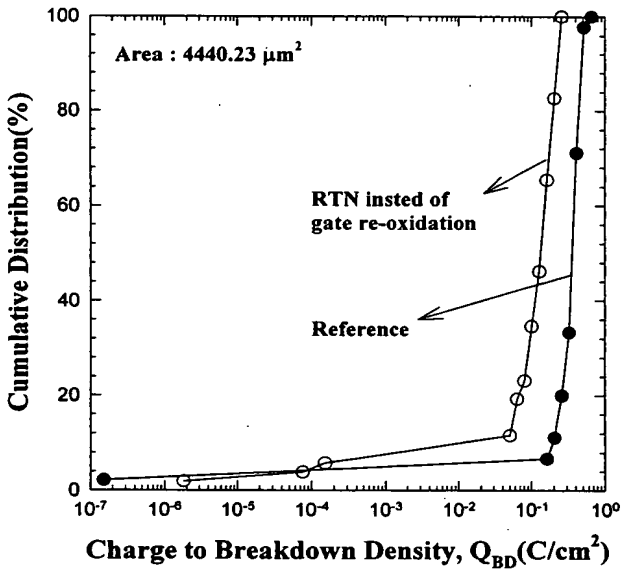


Fig. 10. Reverse-biased leakage current before (filled triangle), after (filled circle) capacitor formation and rapid thermal nitridation (RTN) was applied (open circle) measuring p^+-n junction in an actual sense amplifier (S/A).

the rapid thermal nitridation (RTN) was performed instead of gate reoxidation. Fig. 9 shows (a) the cross-sectional TEM and (b) the plan-view SEM images of STI dislocations when RTN was applied. As depicted in Fig. 9(a), STI dislocations were located at the 0.075 μm depth. Fig. 9(b) shows that STI dislocations were eliminated at the Si surface. Since the junction depth of our device is about 0.12 μm, these results implies that STI dislocations were successfully pinned inside of the source/drain region. Fig. 10 shows the effect of gate reoxidation and RTN on the reverse-biased junction leakage current. When RTN was applied instead of gate reoxidation (open circle), good junction characteristics could be obtained. This result also indicates that STI dislocations could not penetrate the depletion region of pn junction. In order to investigate the gate oxide integrity, charge-to-breakdown density (Q_{BD}) and time-dependent-dielectric-breakdown (TDDB) were measured using the gate edge intensive test pattern, as depicted in Fig. 11. Although Q_{BD} was slightly lowered due to the relatively thinner gate oxide at the gate edge, the result of TDDB measurement indicates that the gate oxide could operate without suffering breakdown over ten years.

IV. Conclusions

When the crystal defects and the mechanical stress are combined under thermal annealing, STI dislocations are generated. An anomalous junction leakage current induced by STI dislocations considerably degrades the refresh characteristics and the standby current of DRAM device. STI dislocations are successfully clamped outside the depletion region of pn junction by judicious control of process-induced defects and mechanical stress. In this work, we have acquired the highly reliable performance of an experimental 16-Mb DRAM with the minimum feature size of 0.15 μm, and this technology can be fairly extensible to the future high-density DRAM devices.



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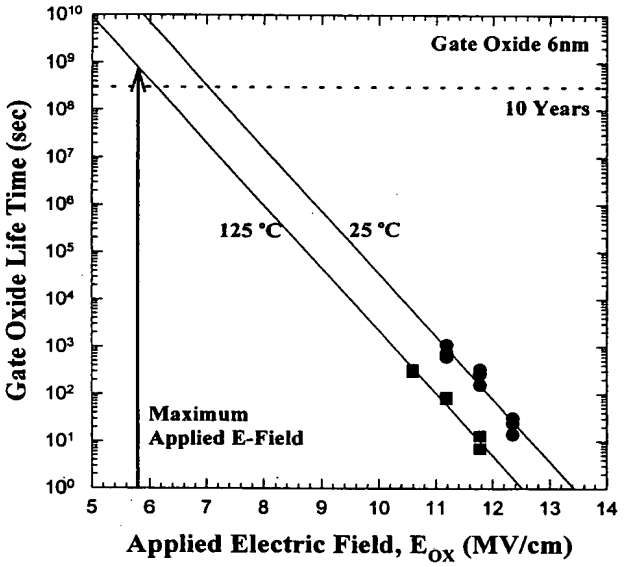

(b)

Fig. 11. Results of (a) charge to breakdown density (Q_{BD}) and (b) time dependent dielectric breakdown (TDDB) measurement using the gate edge intensive test pattern.

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Dr. Kim received the grand prize of the Samsung Group twice for the successful development of 1-Mb DRAM and 1-Gb DRAM in 1986 and 1996, respectively. He is currently a Committee Member of the International Electron Device Meeting (IEDM) and the Korean Semiconductor Symposium (KSC).

Electrical Analysis of Mechanical Stress Induced by STI in Short MOSFETs Using Externally Applied Stress

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***Abstract*—This paper presents an electrical analysis of mechanical stress induced by shallow trench isolation (STI) on MOSFETs of advanced 0.13 μm bulk and silicon-on-insulator (SOI) technologies. By applying external calibrated stress, we present piezoresistive coefficients measurements on these technologies, and we compare small and long transistors electrical responses, evidencing the strong effect of source drain resistance R_{sd}. Then, using the same approach on short devices with different gate-edge-to-STI distances, we quantitatively evaluate stress profile induced by STI and its mean value under the gate of the devices. Results are discussed to explain differences between bulk and SOI technologies, as well as between nMOS and pMOS. We show that the observed higher pMOS drain current shift is related to the process, and may be explained by doping amorphization and recrystallization effects, and not by a piezoresistive coefficient difference as usually assumed.**

***Index Terms*—Doping amorphization and stress, external mechanical stress, piezoresistive response on bulk and silicon-on-insulator (SOI), stress induced by shallow trench isolation (STI).**

I. Introduction

MANAGING internal mechanical stress is a key point to ensure high performance and high reliability in advanced CMOS technologies. Stress can be generated in MOSFET devices at many technological process steps, as they generally imply different process temperature as well as materials with different mechanical properties, thermal coefficient mismatch, and so on [1]. As CMOS devices continue to scale down, these effects become more and more important.

Former studies have demonstrated that mechanical stress can affect workfunction, bandgap, effective mass, and carrier mobility as well as junction leakage [1]. In the case of heterostructures as SiGe devices, stress is used to improve performance [2]. However, the effects of mechanical stress can also reduce the device's performances, and become mainly detrimental: For the back-end part of the process, stress voiding and mechanical weakness of low-κ materials are of prime importance. For the front-end part of the process, shallow trench isolation (STI) is, today, the major source of stress in MOSFET channels [3], [4]. Stress (σ) can also, in the worst case, affect yield through dislocations [5]. It can also induce design dependent nMOS and pMOS drivability [6].

While piezo-resistivity has been deeply studied in bulk silicon for sensors from both theoretical and practical viewpoints, few works have been performed on advanced deep submicrometer CMOS technologies [1]. Stress is difficult to measure locally and is also difficult to simulate, since there is a critical lack of data for many thin-film materials used in technological processes. To optimize the future devices, it is therefore crucial to evaluate the effects of mechanical stress on short channel transistors characteristics.

Based on applying external calibrated stress procedure, this work analyzes electrical effects of mechanical stress induced by STI on MOSFETs of 0.13-μm bulk and silicon-on-insulator (SOI) technologies. We show how to evaluate stress profile induced by STI and its mean value under the gate of the devices. Both nMOS and pMOS are studied as well as devices with different gate oxide thicknesses. Results are discussed and allow us to explain differences observed in bulk versus SOI and nMOS versus pMOS.

II. Tested Devices

Devices are n- and pMOS transistors fabricated on (001) silicon substrates, for bulk and partially depleted (with buried oxide: 400 nm and silicon film: 150 nm) SOI 0.13-μm CMOS technologies. Process options with high internal stress (HS) or low internal stress (LS) by liner (trench oxidation after STI process) optimization were tested, as well as core devices (GO1) with gate oxide thickness $T_{ox} = 2$ nm and high-voltage devices (GO2) with gate oxide thickness $T_{ox} = 6.5$ nm. Process of GO1 and GO2 were very similar except for T_{ox}, V_t adjust, nominal length of 0.13 and 0.35 μm, respectively, and slight source/drain implant adjustment.

GO1 tested devices have a gate length $L = 10$ μm (long devices) or $L = 0.13$ μm (short devices). GO2 tested devices have a gate length $L = 10$ μm (long devices) or $L = 0.35$ μm (short devices). The STI-to-gate-edge distance (hereafter called "a" parameter) varies from 0.34 to 10 μm. For all devices the gate width is $W = 10$ μm.

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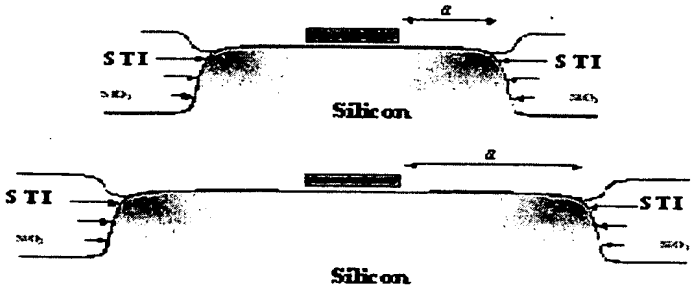

Fig. 1. Schematic of mechanical stress induced by STI on bulk transistors. Stress depends on "a" parameter. Arrows indicate main stress direction.

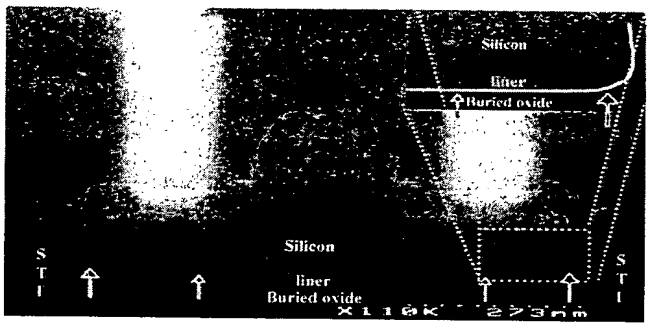

Fig. 2. Cross-sectional SEM picture for pMOS SOI device (HS) with $L = 0.13$ μm: Effect of the liner on the corners of the silicon layer; observation of silicon curvature.

III. Stress Induced by STI

The STI process can induce significant mechanical stress in devices. Due to the trench oxidation (liner), difference in thermal expansion coefficient between Si and SiO_2 and visco-elastic effects during thermal anneals, a compressive stress develops (Fig. 1). For SOI, silicon can reoxidize at the buried-oxide/Si interface at the STI edge, bending silicon and adding a stress component (Fig. 2), which is compressive inside the channel of the transistor [4], [6].

Through piezoresistive effects, electrical parameters (i.e., mobility, threshold voltage, etc.) are modified. A decrease of nMOS current and an increase of pMOS current are observed with increasing compressive stress. The higher the STI-to-gate-edge distance ("a" parameter), the lower the compressive stress (Fig. 3). The unstressed reference is taken at $a = 10$ μm. The relationship is not linear, as the back interface of the wafer acts as a free surface and tends to impose a zero stress. This leads to an attenuation of the stress with a characteristic length of around 1.5 μm. Notice that this characteristic length will strongly depend on trench geometry, especially on trench depth.

Taking into account the STI effect in the direction of the width, and on the length of the transistor, real device stress repartition is highly three-dimensional. For the present paper, all the tested transistors have $W = 10$ μm, and a bidimensional approach is a good approximation. As can be seen in Fig. 3, different process scenarios highly modify stress values. Low stress (LS) SOI process shows much lower $I_d(a)$ variation than high stress (HS) SOI process. For practical reasons, most of the measurements have been performed on HS process.

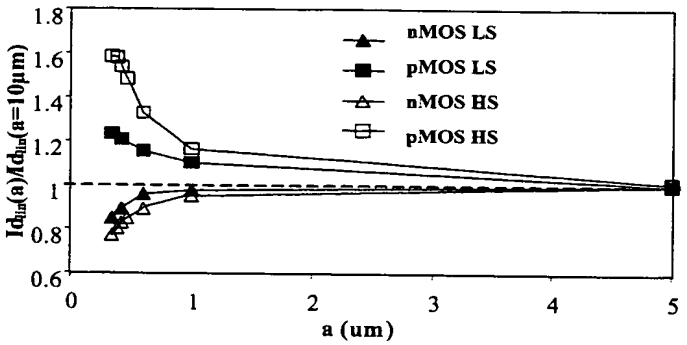

Fig. 3. Relative $I_d(a)$ variations of SOI low-stress (plain symbol) $L = 0.13$ μm and high-stress devices (open symbol) $L = 0.13$ μm SOI.

IV. Experimental Method

A four-point bending technique is used to apply an external calibrated mechanical stress on MOSFETs in rectangular strips cut from the wafer. The interest of this method is to generate a uniform uniaxial stress between the two central fulcrums if the configuration shown in Fig. 4(a) is respected.

The devices are defined on (001) silicon and the mechanical stress σ is applied parallel to the wafer surface along $\langle 110 \rangle$ silicon direction [Fig. 4(a)]. The surface stress is calculated from the relationship [7],

$$\sigma = \frac{12Eyt}{4l^2 - 3L^2} \tag{1}$$

where E is Young's Modulus ($E = 168$ GPa for $\langle 110 \rangle$ silicon orientation), y is the total strip vertical deformation (measured by a micrometer screw), t the total thickness of the strip, L is the length of the strip between the two external fulcrums and l is equal to $L/4$.

The transfer characteristics of the devices were monitored using a semiconductor parameter analyzer (HP 4155). The estimated error is mainly due to the uncertainty of y measurement, true E value, quality, and reproducibility of contact probe/pad. The global accuracy in our setup is estimated to be around 7%.

In the four-point-bending apparatus, rectangular strips are cut from the wafer by a saw technique and placed in the bending rig to generate the desired mechanical stresses. With an appropriate preparation of the strips, a mechanical stress can be applied in either the longitudinal (parallel to the current flow) or transverse directions (perpendicular to the current flow). As most strips of silicon fail for a mechanical stress around 175–220 MPa, we keep the applied mechanical stress below 130 MPa in our experiments. Compressive or tensile stress can be applied. In all cases, a continuous linear variation of parameters from compressive to tensile stress was observed [Fig. 4(b)]. For practical reasons, we will refer mainly to tensile stress. For full piezo-resistance analysis, stress was applied in a longitudinal or a transversal direction (by appropriate sample preparation).

Simulations were performed to calibrate the method. In particular, Fig. 5 shows that externally applied stress in the MOS channel is similar for bulk and SOI for a given wafer thickness; buried oxide has a negligible influence on surface stress. This means that the stress is mainly imposed by the thick bulk Si part

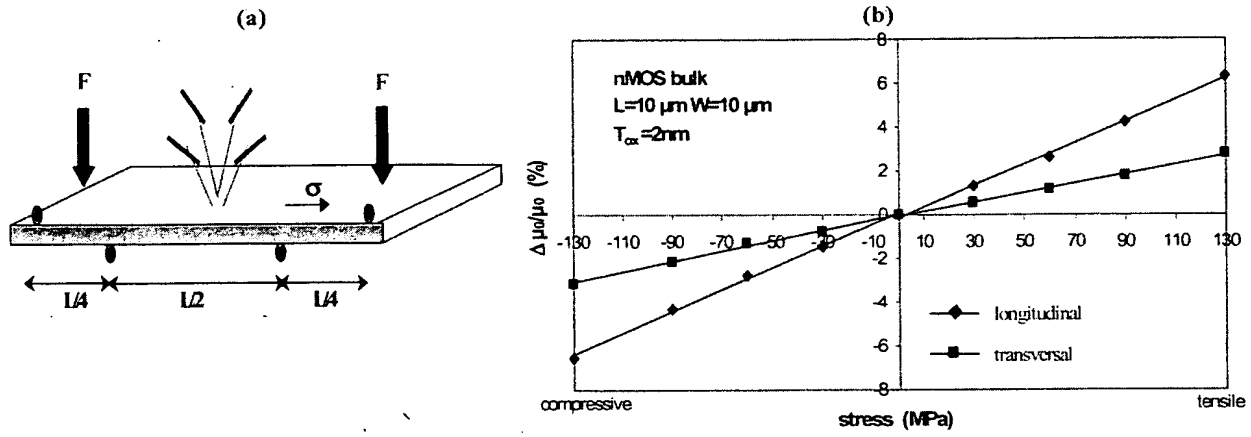

Fig. 4. (a) Four-point-bending method. Configuration for tensile stress. F applied through micrometer screw. (b) Continuous linear variation of parameters from compressive to tensile stress was observed for all devices (illustration for a nMOS bulk G01).

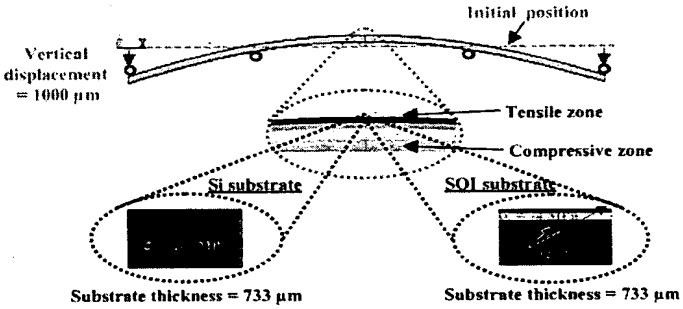

Fig. 5. Simulation of externally applied stress in MOS bulk and SOI channels. Note the negligible influence of the buried oxide.

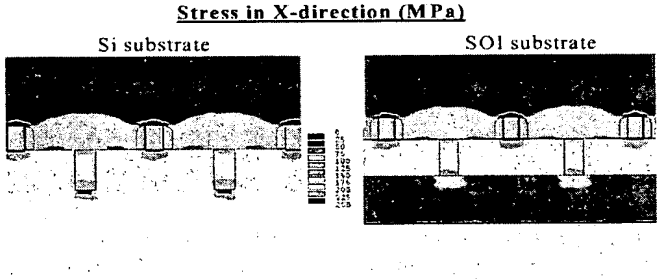

Fig. 6. Two-dimensional mapping of simulated stress in the X direction during wafer bending, for bulk and SOI devices with STI. It shows that the expected stress is obtained under the gate of transistors and that only zone under STI is modified.

of the wafer. Another study (Fig. 6) shows that the same external applied stress under the gate by bending is not modified by the vicinity of STI (and of buried oxide). Applied stress by bending method inside the channel of our SOI devices with STI is then reasonably well controlled.

V. Piezoresistive Effects on Long and Small Transistors

We first investigated piezoresistive effects on internal stress free (that means no internal stress induced by STI) devices. In this case, gate-edge-to-STI distance (a) is large (10 μm) and STI-induced stress does not modify electrical characteristics of the devices. Piezoresistive study is performed to ensure a deep enough understanding of stress effects on electrical characteristics of the devices, that all geometries behave in an understandable way, and to give references for the analysis of devices with STI internal stress. Study and results on these internal stress-free devices have been presented and discussed in [8], and only main conclusions are given here for clarity of further paragraphs. All measurements were performed at $|V_d| = 0.1$ V.

A. Long Transistors

We tested 10-μm-long devices and explored the dependence of the electrical characteristics versus mechanical stress. An external homogeneous stress ranging from 0 to 130 MPa was applied. The following usual results were obtained [8]: threshold voltage variation has been found negligible (theoretical calculations predict a variation less than 3 mV for a stress equal to 130 MPa) while mobility was the main varying parameter. These results are consistent with previously reported studies [9].

Example for nMOS (pMOS) mobility variations is given in Fig. 7(a) and (b) for bulk and SOI devices. Excellent linear dependencies versus σ are observed. The slope of the curves corresponds to the piezoresistive coefficient. Table I gives all the piezoresistive coefficients for nMOS and pMOS and for longitudinal and transverse stress. Results show general tendencies already reported on previous generations of technologies [9], [10]: For nMOS, $\Delta\mu_0/\mu_0$ increases (decreases) under tensile (compressive) stress in a more pronounced way in the longitudinal direction than in the transversal one. For pMOS, $\Delta\mu_0/\mu_0$ decreases (increases) under a longitudinal tensile (compressive) stress and increases (decreases) under a transversal tensile (compressive) stress. In the case of nMOS, these phenomena are theoretically explained by variations of effective mass of carrier induced by change of carrier populations in the transverse and longitudinal valleys. In the case of pMOS, it is mainly explained by modification of populations of light and heavy holes added to modification of band shape [11].

B. Small Transistors

Similarly to long transistors, threshold voltage variation versus mechanical stress has been found negligible on small

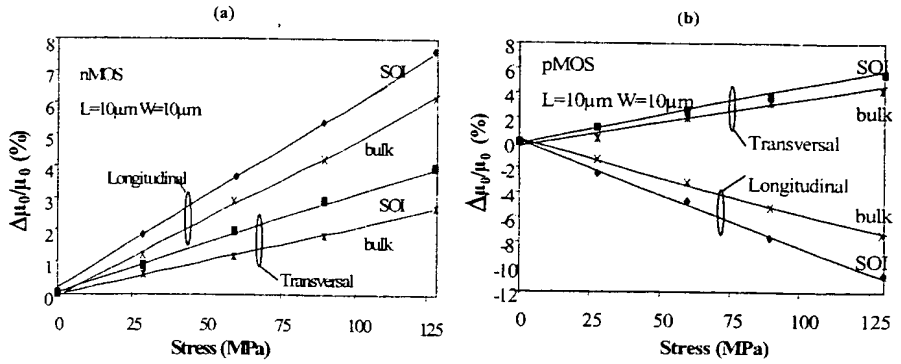

Fig. 7. Normalized mobility change versus applied uniaxial tensile stress for bulk and SOI long channel devices. (a) nMOS case. (b) pMOS case.

TABLE I
PIEZORESISTANCE COEFFICIENTS OBTAINED FOR BULK AND SOI $L = 10\ \mu m$ DEVICES ($\times 10^{-12}$ Pa^{-1}) WITH G01 AND G02. ERROR ESTIMATION: $\pm 60.10^{-12}$ Pa^{-1}. Π_L IS THE LONGITUDINAL COEFFICIENT Π_T IS THE TRANSVERSAL COEFFICIENT

G01	bulk	SOI	G02	bulk	SOI
Π_L^{nMOS}	485	580	Π_L^{nMOS}	495	497
Π_T^{nMOS}	212	311	Π_T^{nMOS}	262	230
Π_L^{pMOS}	-600	-767	Π_L^{pMOS}	-571	-648
Π_T^{pMOS}	383	422	Π_T^{pMOS}	376	466

TABLE II
CORRECTION OF PIEZORESISTANCE COEFFICIENTS FOR PMOSFET/SOI WITH $L = 0.13\ \mu m$ ON (001) SILICON ($\times 10^{-12}$ Pa^{-1}). ONCE CORRECTED (ERROR ESTIMATION: $\pm 100.10^{-12}$ Pa^{-1}), MAIN COEFFICIENTS ARE CLOSE TO THOSE OF LONG CHANNEL PRESENTED IN TABLE I

MOSFET parameters	Measured values	Corrected values	Estimated Error
Channel length	0.13 μm		
Parasitic R_{SD}	35 Ω		
V_d	-0.1 V		
Π_L ($.10^{-12}Pa^{-1}$)	**-372**	**-561**	+/- 100
Π_T ($.10^{-12}Pa^{-1}$)	**431**	**469**	+/- 100

transistors. On short-channel devices ($L = 0.13\ \mu m$), piezoresistive longitudinal coefficient Π_L is significantly lower than for $L = 10\ \mu m$ (see Table II). Most of this difference has been explained by a source/drain resistance (R_{sd}) attenuation effect. R_{sd} extraction was performed by Taur's technique [8], [12] and no R_{sd} variations versus stress were observed. Notice that R_{sd} extraction is difficult on these very small transistors: Slight variations with stress can then be hidden by extraction errors. Once corrected from source/drain resistance, and taking into account measurement errors, piezoresistive coefficient calculated from the intrinsic low field mobility of the short device is close to that of long device [8] (see Table II). This key point indicates first that fundamental behavior of small and long devices is the same, and second, that differences of device topologies between short and long do not play a major role in absorbing or enhancing locally the externally applied stress. Similarly, local or two-dimensional (2–D) stress (induced at the gate edge, at junctions, etc.) does not affect significantly short devices as compared to longer ones. The same results are obtained on GO2 devices.

While not evidenced through parameter extraction, part of the remaining difference might be attributed to source/drain correction which has been supposed constant versus applied stress. Source/drain resistance is composed of different contributions, namely metal–silicide contact resistance, silicide resistance, and lightly doped drain (LDD) resistance. Variations of the first two contributions versus σ should be negligible. LDD resistance variation versus σ is still questionable. It is well known that the higher the doping level, the lower the piezoresistive variation. In this way, the lower doped part of the LDD may play a role in the results of short devices. It will be evaluated in future work.

While the previous analysis of mobility gives the necessary electrical understanding for the stress evaluation developed in the next section, it must be emphasized that current drivability is a more important parameter for circuits applications. Depending on geometry and measurement conditions, saturation current variations with stress are generally found from similar to half that of linear current variations [10], [13]. This should remain true in future technologies, as other studies [14] have shown experimentally that mobility and velocity variations with stress are correlated even near ballistic operation.

VI. STRESS EVALUATION BY BENDING

A. SOI Devices

The bending method was applied for $L = 0.13\ \mu m$ pMOS and nMOS HS SOI with various gate-edge-to-STI "a" distance. For each device, a tensile stress from 0 to 130 MPa was applied. Two main results can be pointed out:

First we can observe in Fig. 8 that these devices with various "a" have parallel $I_d(\sigma)$ curves even if they have very different internal σ_0. The order of magnitude of σ_0 variation is clearly over 1 GPa as varying "a" from 10 to 0.34 μm changes the current from around 50%, while applying 130 MPa changes the current by around only 3%. Parallel $I_d(\sigma)$ is a fundamental result which indicates that the different sources of stress considered here, namely due to STI and due to bending, are additive and prove a common unique law $I_d(\sigma_0 + \sigma)$ in a stress range well above 1 GPa. As shown in Figs. 9 and 10, we can then reconstruct the $I_d(\sigma)$ curve on a wide range of stress, and avoid errors due to long range extrapolations. No nonlinearity, relaxation effects, etc., are noticed.

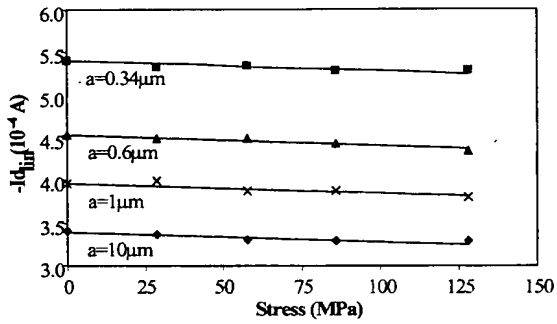

Fig. 8. Four-point bending experiment on pMOS SOI G01 HS with varying gate-STI distance "a." Analysis of parallelism.

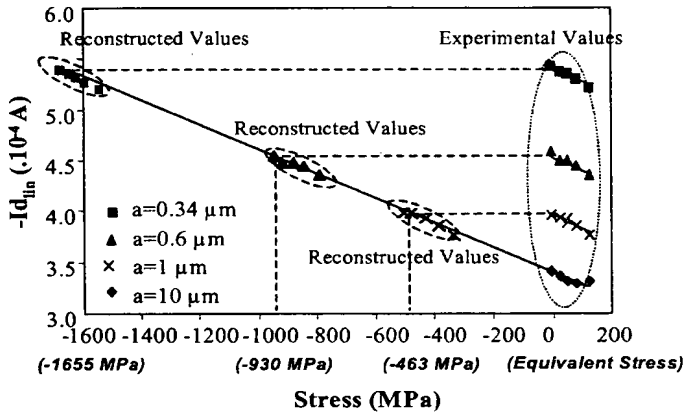

Fig. 9. Four-point bending experiment on pMOS SOI G01 HS with varying "a." This graph shows how parallel curves allow for reconstruction of the extrapolation curve. Internal stress extrapolation.

Second by exploiting the observed linearity and curves parallelism, we can extrapolate for pMOS (Fig. 9) and for nMOS (Fig. 10) the curve of "zero stress" transistor, $a = 10$ μm, on which external stress is applied, to recover the I_d value of devices without external applied stress, but with STI-induced internal stress σ_0. This procedure can be considered valid as long as STI-induced stress is homogeneous along the channel of the transistor. This is considered to be true for these $L = 0.13$ μm devices as this length is small, compared with the 2-D behavior of the stress, which extends to $\sim$ 1.3 μm [4], [6]. For GO2 devices ($L = 0.35$ μm), the error should be more significant and results will be analyzed in a qualitative way. The stress in the channels obtained for the different "a" values is shown in Fig. 11. This curve gives a realistic quantitative 2-D stress profile versus "a" distance. The maximum value obtained for $a_{\min}$ is around -1655 MPa for pMOS SOI and around -756 MPa for nMOS SOI.

B. Bulk Devices

Stress profiles for bulk pMOS and nMOS devices are shown respectively in Figs. 12(a) and 13(a). We observe profiles similar to the SOI case, but with much lower equivalent stress values. Moreover, stresses around -400 MPa are in this case rather similar for both nMOS and pMOS.

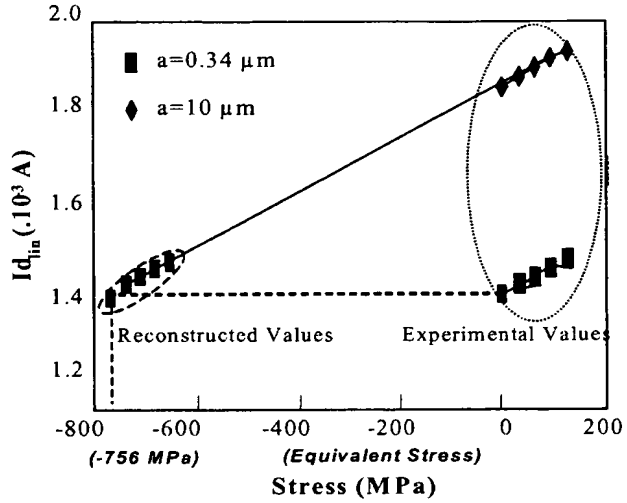

Fig. 10. Four-point bending experiment on nMOS SOI G01 HS with varying "a." Internal stress extrapolation.

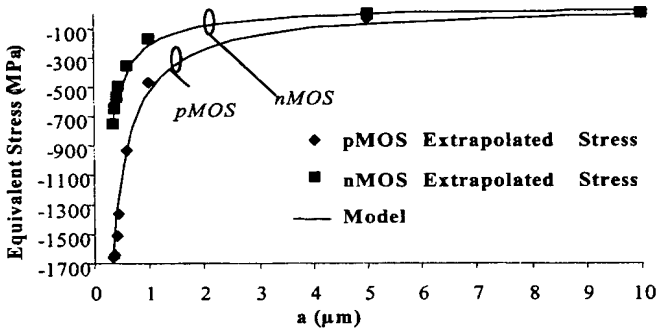

Fig. 11. Stress profile for $L = 0.13$ μm devices (experimental results and model fitting, performed on nMOS and pMOS SOI transistors [6]).

C. GO1 versus GO2 Devices

The main result here is that in all cases, profiles and values of stresses of GO1 are similar to that of GO2 for each kind of devices (Figs. 12 and 13). This is true in spite of small differences and previously mentioned restrictions in the stress evaluation of GO2 devices. Similar values of stress for GO1 and GO2 devices, featuring significantly different oxide thicknesses, confirm a weak impact of the gate stack on channel stress. A second observation is that while GO1 and GO2 stresses are practically identical for pMOS, GO2 stress is slightly higher for GO1 than GO2 for nMOS. This is true for both SOI and bulk devices.

VII. Discussion

A. Bulk versus SOI

For the studied devices, it means that higher stress in SOI is due to thin silicon layer deformation due to oxidation as explained previously on Fig. 2. Stress induced by active area curvature due to the oxidation of the interface buried oxide/silicon can be estimated around -1 GPa. For our HS devices, this component adds to lateral "classical" stress effect of STI. Both stresses are compressive and similarly oriented. This extra component of stress in SOI devices can be reduced by liner process modification as seen on Fig. 3 (LS process).

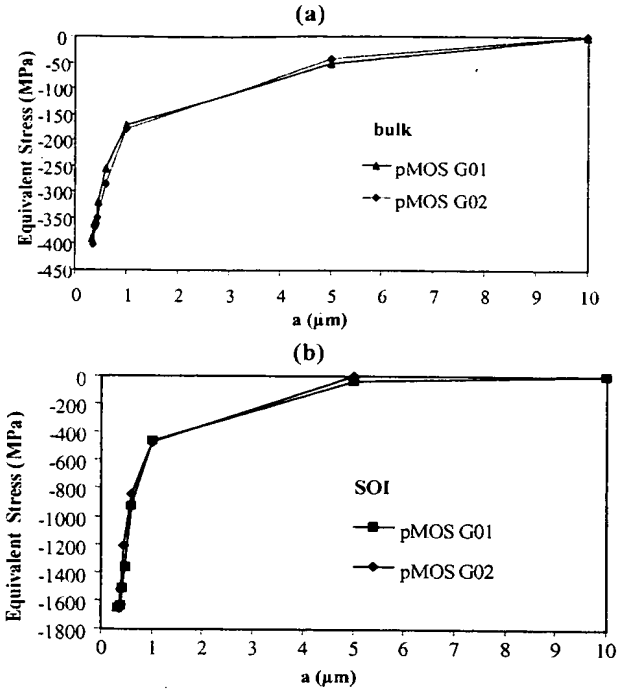

Fig. 12. Stress profile obtained for experimental results on G01 (L = 0.13 μm) and G02 (L = 0.35 μm) for (a) pMOS bulk and (b) pMOS SOI HS.

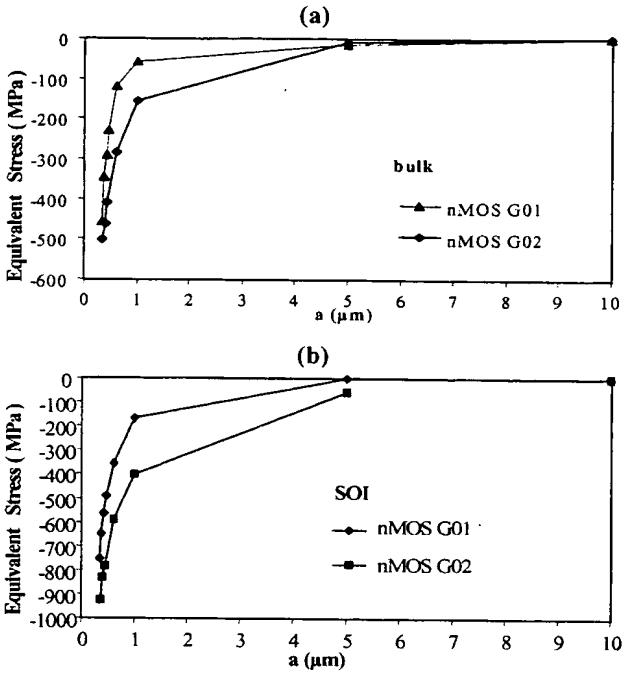

Fig. 13. Stress profile obtained for experimental results on G01 (L = 0.13 μm) and G02 (L = 0.35 μm) for (a) nMOS bulk and (b) nMOS SOI HS.

B. nMOS versus pMOS

An important result of the previous study is that the higher stress effects observed on pMOS compared to nMOS for SOI devices (see Fig. 3) are not due to piezoresistive coefficient differences but rather to different internal stress σ_0. Among the possible causes of this difference are STI sidewall oxidation, silicide stress, different doping, etc. However, during STI process steps, there should be no oxidation difference (doping implant is not yet performed) and no difference between SOI nMOS and pMOS curvature should exist, as observed by scanning electron microscope (SEM) at these steps. Silicide stress on n^+ and p^+ junctions is also believed to be low. Implantation process and more precisely the full sequence implantation/amorphization/recrystallization may be the cause of the nMOS/pMOS difference. It is well known that amorphous Si relaxes by viscous flow under compressive stress with a temperature dependence. This relaxation is driven by the decrease of concentration of structural defects [15].

The following explanation is then proposed: The silicon is amorphized significantly during Arsenic n^+ implant on nMOS ($2\ 10^{15}$ cm^{-2}; no pre-amorphization implant, amorphization $\sim$ 50 nm) so that σ_0 may significantly relax during the subsequent thermal treatments and recrystallization. σ_0 relaxes from -1650 MPa to about -750 MPa in the case of nMOS. On the other hand, the silicon is not amorphized with usual Boron P+ doping on pMOS ($2\ 10^{15}$ cm^{-2}; no pre-amorphization implant; amorphization $\sim$ 0 nm), and no σ_0 relaxation can occur. As a consequence, pMOS have higher σ_0 than nMOS, even if they share the same STI process. Notice that a similar and complementary relaxation effect may occur due to the degradation of the silicon dioxide STI due to Arsenic and Boron implantation.

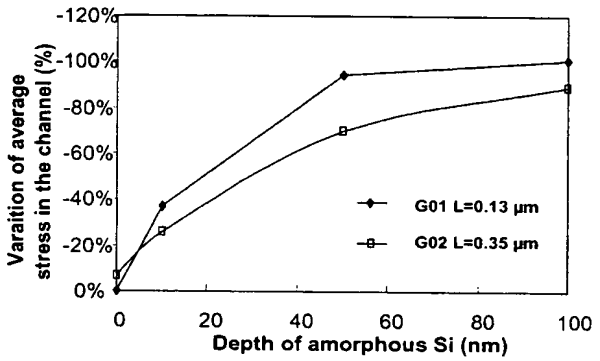

Fig. 14. Simulation of variations of average mechanical stress in the channel versus depth of amorphized silicon. The stress along the current flow is evaluated for the case G01 (L = 0.13 μm) and the case G02 ($L \cong$ 0.35 μm). Simulations where performed after implantation (spike anneal step) and correspond to "extreme case:" amorphized layer is supposed to completely absorb the stress during recrystallization of silicon (equivalent to Young's Modulus E$\sim$0 GPa).

In the case of bulk devices, stresses are believed to be weak enough after STI ($\sim$, -400 MPa) so that no significant relaxation occurs during recrystallization. NMOS and pMOS keep their initial stress level.

In order to support this hypothesis, we performed complementary mechanical simulations with varying depths of amorphized silicon, from 0 to 100 nm. As we do not have data about the mechanical behavior of our amorphized layer, we simulated an "extreme case," with a layer able to completely absorb stress during recrystallization (Fig. 14). For our case, (50-nm amorphization), it appears that up to 94% of the average stress in the channel is then relaxed. In the real case, the amorphized layer does not completely absorb the stress during recrystallization; this should explain the experimental average stress value of -750 MPa corresponding to 55% of relaxation.

C. GO1 versus GO2

Previous discussion was confirmed by GO1 and GO2 device analysis: pMOS GO1 and pMOS GO2 showed exactly the same level of stress [Fig. 12(a) and (b)]: Source/drain doping was identical, and did not modify stress by amorphization. NMOS GO1 showed slightly lower stress than nMOS GO2 [Fig. 13(a) and (b)]: This was explained partly by a slight extra arsenic implant on GO1, which induced more amorphization and σ_0 relaxation, partly by the longer size of the transistor GO2 which induced a reduced average stress relaxation in the channel by bidimensional effects ("extreme case" simulations calculated 69% compared to 94% for GO1).

VIII. Conclusion

Using a four-point bending method, we have extracted valuable information on piezoresistance and on stress effects for advanced 0.13-μm bulk and SOI technologies. We have assessed the stress response on short transistors. Stress profile induced by STI has been extracted leading to a better understanding of the differences between bulk and SOI technologies, as well as between nMOS and pMOS devices. Higher pMOS drain current shifts are usually observed relatively to nMOS and are due to the difference of technology process leading to different stress. A convincing hypothesis for this difference is stress relaxation in the case of nMOS due to amorphization and recrystallization.

Such methodology and data can have many further applications in the field of simulation calibration [6] and of electrical analysis of parameters dependence with stress. These results help to understand, minimize or optimize internal stress effects induced during the process.

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Dr. Ghibaudo was or is a member of several technical/scientific committees of International Conferences (ESSDERC 1993, WOLTE, ICMTS, MIEL 1995-2004, ESREF 1996, 1998, 2000, 2003, SISC, MIGAS, ULIS, IEEE/IPFA). He was co-founder of the First European Workshop on Low Temperature Electronics (WOLTE '94) and organizer of eight Workshops/Summer Schools during the last ten years.

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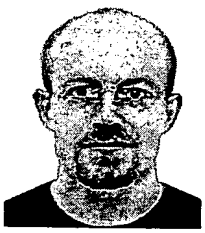

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Finite Element Optimization of a MOSFET Structure : The Role of Interlayer Material for Residual Stress Reduction

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ABSTRACT

Mechanical stress induced degradations of a MOS technology are investigated. Bidimensional stress simulations, coupled with electrical characterizations reveal the importance of the gate formation and TEOS deposition steps in the generation of mechanical stress. The use of a doped oxide as interlayer material between the polysilicon gate and the TEOS film is shown to significantly reduce the residual stress and associated electrical failures.

INTRODUCTION

Modern integrated circuit processes involve a large variety of materials, having very different mechanical properties. Unfortunately, the discontinuities are responsible for stress generation, as a result of any thermal or mechanical loading, affecting significantly the electrical characteristics of the devices. This problem is here addressed through the optimization of a BIMOS technology, including vertical DMOS. The study is based on process simulations and electrical characterizations. For this purpose, an homogenous and advanced stress simulation system has been implemented in the process simulator IMPACT-4 [1], allowing the evaluation of the cumulative mechanical stresses (i.e., induced by oxidation, thermal cycling and material deposition/etching) at each process steps. Experimental measurements giving the variation of the stress as a function of temperature provide the data for calibration. These new capabilities are used to analyse the origin of the observed electrical degradations for the DMOS structure and an original solution, based on the role of an interlayer joint, is proposed and validated.

FABRICATION PROCESS

Fig. 1 summarizes the main steps of the process flow for the MOS device. Epitaxial 10 Ohm/cm P-type (100) silicon wafers were used as starting material. The electrical isolation was obtained with a LOCOS structure (1000 °C - 0.7 µm thick). After the growth of the gate oxide (50 nm), an undoped polysilicon, 500 nm thick, was deposited by LPCVD, then phosphorus doped and anisotropically etched to form the gate. The drive-in of the implanted layers was followed by a LPCVD TEOS deposition, performed in two steps, 400 nm thick in total. Finally, after the densification and passivation steps, the contact holes were etched and filled with aluminium.

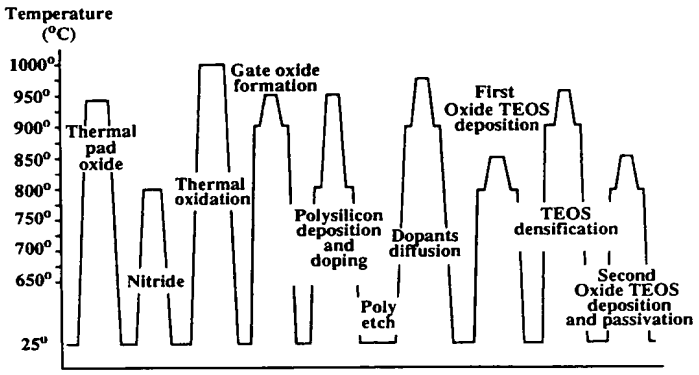

Figure 1: Description of the main thermal cycles and topological changes of the BIMOS process flow, describing the simulation input.

NUMERICAL MODEL AND CALIBRATION

Based on the Finite Element Method, a general calculation system of the fabrication induced stresses has been implemented in IMPACT-4. The deformation of all the layers is calculated by applying the equilibrium forces conditions to the entire structure, the initial strain conditions at each time step being the superposition of the thermal, intrinsic and residual (i.e., accumulated from previous steps) components. The stress-strain relationships are considered purely elastic for silicon and polysilicon, while non-linear (Eyring) viscoelastic behavior is adopted for nitride, thermal and deposited oxides [2].

The mechanical properties of the thermal oxide have already been calibrated [2]. Using standard values of the thermal expansion coefficient (i.e., 4.5 10^{-6} /°C - 0.5 10^{-6} / °C for Si and SiO_2, respectively), the simulation of the oxide stress variations as a function of temperature for a Si/ SiO_2 bilayer gives a good agreement with experiments [3] and confirms the validity of the previous calibration as shown in Fig. 2. In a first order approximation, one can consider that undoped deposited oxide possesses the same mechanical properties as thermal oxide. However, doped deposited SiO_2 exhibits a lower viscosity than thermal oxide [4]. This viscosity is calibrated by simulating the cooling of a densified P-doped APCVD SiO_2 film (Fig. 3) [5]. The experimental variation of stress versus temperature shows a viscoelastic regime for temperature as low as 700°C. This behavior is correctly reproduced using the calibrated values of viscosity reported in Fig. 4. For T< 300°C,

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the variation of the stress softens up at relatively small values, which is typical of plastic deformation. This phenomenon is modeled by the decrease of the shear stress threshold (2kT/VP) in the Eyring's model of viscosity.

Finally, intrinsic stresses at the deposition temperature are extracted by subtracting the simulated thermal stress, from the measured total film stress.

MECHANICAL ANALYSIS

The MOS fabrication, including isolation steps, has been simulated with IMPACT-4 and the results before the contact hole etching are given in Fig. 5, exhibiting high stress peaks both in the bird's beak region and in the active area. However, since the electrical measurements indicate the existence of junction leakage currents in the vicinity of the gate edge, the mechanical optimization has been focused on the gate formation and TEOS deposition steps.
First, the influence of the intrinsic stress in polysilicon has been investigated. Fig. 6 compares the stress level for two simulated structures having a) a compressive stress of -500 MPa (calibrated value) and b) no intrinsic stress. The results confirm the disastrous effect of the intrinsic component which generates high tensile and compressive stress in the active area (Fig. 6a) while the thermal component has a lower influence (Fig. 6b). Furthermore, the simulations confirm that intrinsic stress is also responsible for the increase of stress in silicon as the gate length become wider (Fig. 7), results which can not be justified by thermal cycling [6]. The nature (either compressive or tensile) of residual stresses developed during cooling of the TEOS deposition steps is illustrated quantitatively in Fig. 8. Before TEOS deposition, the polysilicon gate is only constrained on one edge (oxide/polysilicon interface) and its stress is essentially compressive (Fig. 8a). During TEOS deposition, the polysilicon gate is expanded (ramp-up), then covered by the TEOS oxide and finally experiences large thermal mismatch (ramp-down) due to the high stiffness of the TEOS oxide which prevents large deformation of the structure (Fig. 8b). Consequently, in order to reduce this residual stress, the use of an interlayer material is proposed : TEOS oxide and polysilicon have been joined using a doped oxide interlayer, instead of a direct bonding (Fig. 9). According to simulation results, this doped oxide, much more viscous and plastic than the TEOS oxide, can significantly reduce the stress peak (Fig. 10), as a result of its extensive localized deformation.

EXPERIMENTAL RESULTS

Above results of simulation have been confirmed by the following experiments. Power DMOS transistors, with self-aligned source and backgate junctions, have been processed (Fig. 11) with two types of LPCVD oxide insulating layers : 400 nm undoped TEOS oxide versus 100 nm BPSG covered by 300 nm undoped TEOS oxide. The cells had an octogonal shape with half of the sides being parallel to <110> crystalline directions. The device was sized to deliver 1 A drain current. The devices containing BPSG have been found free of dislocations (as deduced from TEM observations) and exhibit a leakage current of the order of 100 pA (measured at VDS=10V), whereas the devices that did not contain BPSG exhibit dislocation loops in 5% of the cells (in <110> planes, along the <110> polysilicon edges), together with a total leakage current of the order of 10mA (Fig. 12).

CONCLUSION

A mechanical optimization of the MOSFET devices of a BIMOS technology has been performed by extensive use of the calibrated stress simulation capabilities of the process simulator IMPACT-4. It was confirmed by electrical measurements that the use of interlayer joint is very efficient to control residual stress. This principle could be extended to other dissimilar material-joining problems such as trench isolation where polysilicon is embedded in a thermal oxide matrix.

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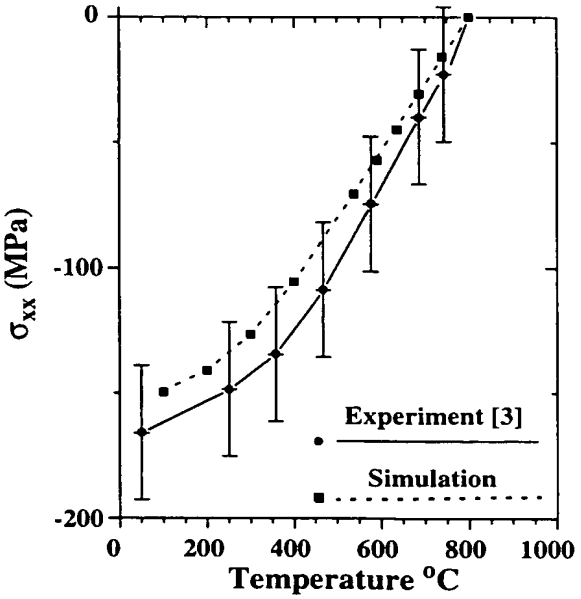

Figure 2: Stresses induced by the cooling of a thermal oxide layer. Measurement suffers an average error of 60MPa.

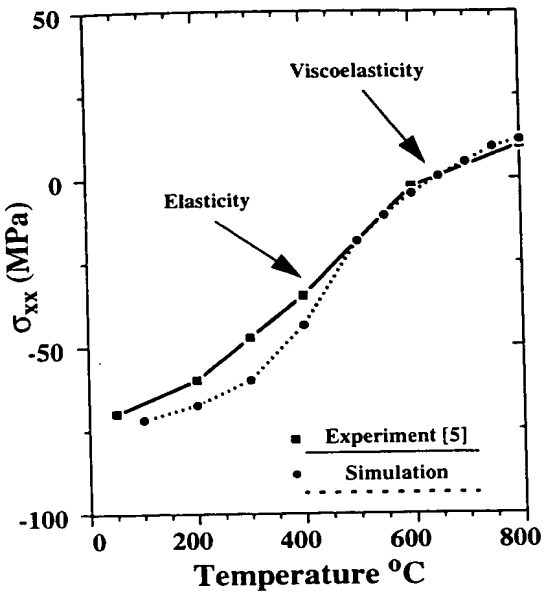

Figure 3: Silicon stresses induced by the cooling of a doped APCVD oxide layer.

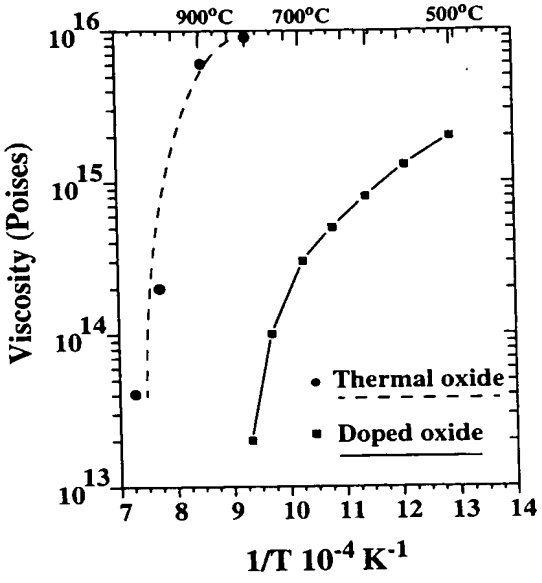

Figure 4: Calibrated viscosities for doped APCVD oxide. Previous calibration of thermal oxide is given for comparison.

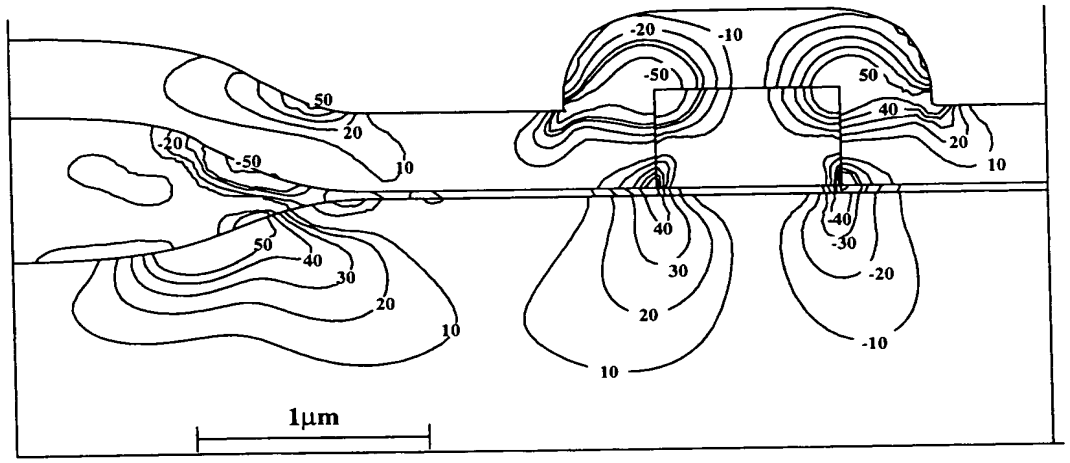

Figure 5: Simulation of the MOS structure before the contact holes etching with the corresponding shear stresses in MPa.

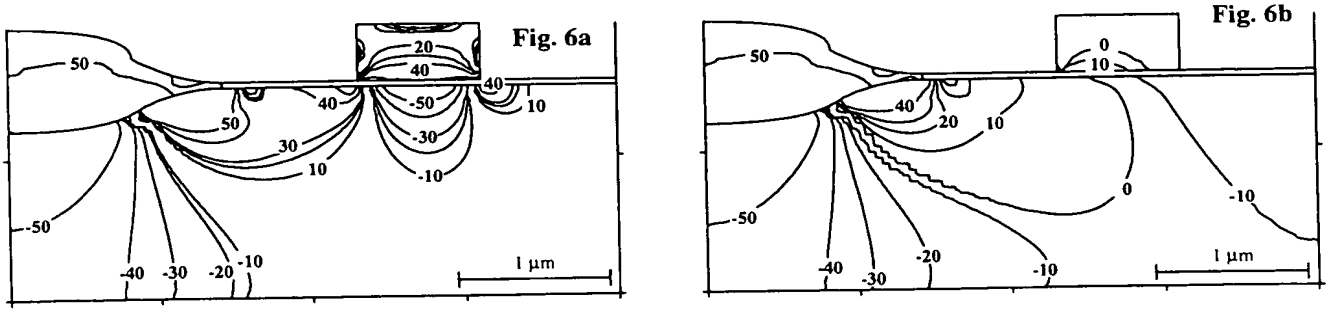

Figure 6: Influence of the polysilicon intrinsic stresses on the pressure distribution: a) simulation with compressive intrinsic stresses for the polysilicon gate, b) without intrinsic stresses.The isovalues are given in MPa.

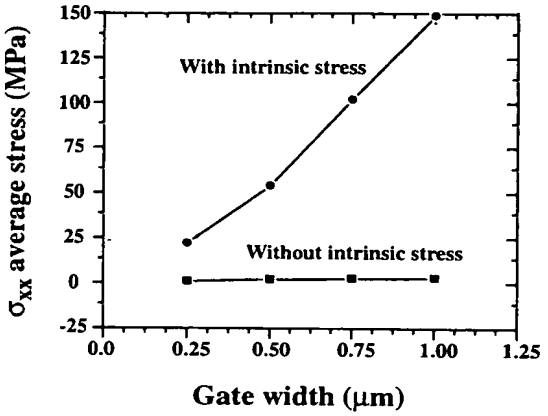

Figure 7: Polysilicon gate width effect on the average stress under the active area.

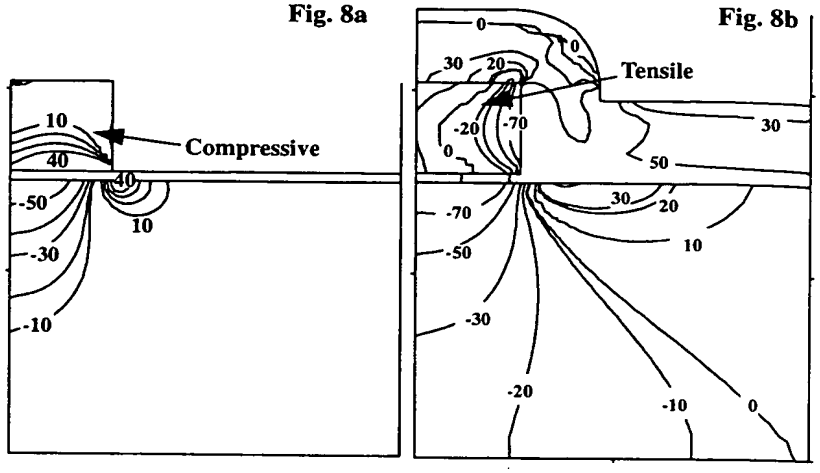

Figure 8: Simulated structures, a) after the gate formation, b) after the TEOS insulating layer deposition. The pressure distribution is given in MPa.

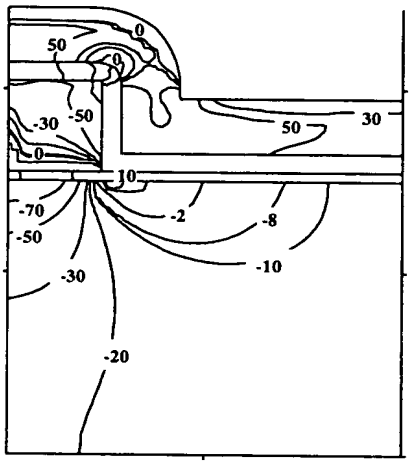

Figure 9: Simulation result of the final structure using a BPSG interlayer (100nm thick). The pressure distribution is given in MPa.

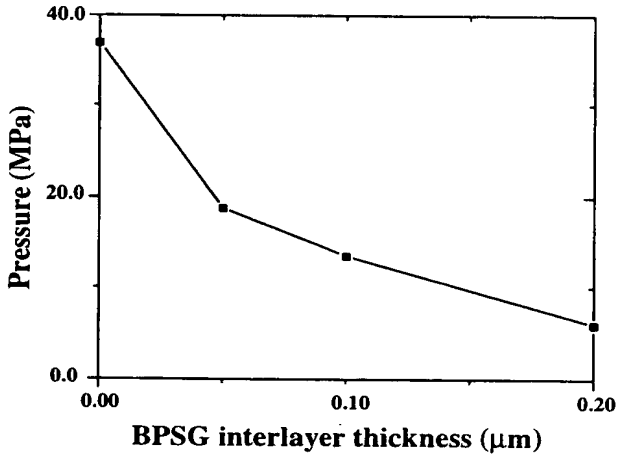

Figure 10: Reduction of the maximum compressive stress in silicon (near the gate edge) for different BPSG oxide layer thicknesses.

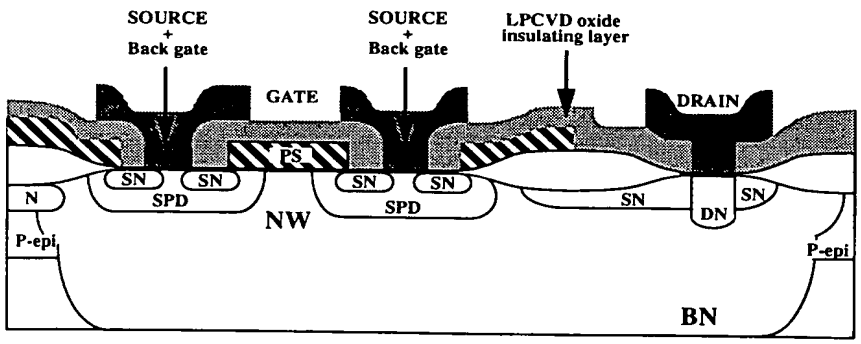

Figure 11: Schematic cross section of the VDMOS transistor.

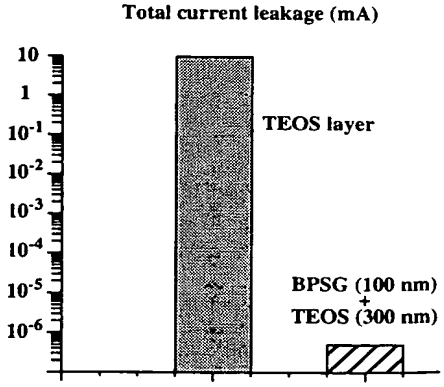

Figure 12: Measured leakage current for the DMOS structures processed without or with a BPSG interlayer.

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Electrical Analysis of Mechanical Stress Induced by Shallow Trench Isolation

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Abstract

This paper presents an electrical analysis of mechanical stress induced by Shallow Trench Isolation (STI) on MOSFETs of advanced 0.13µm SOI technology. By applying external calibrated stress we measure piezoresistive effects and compare small and long transistors electrical responses. Main results are the mobility variations with stress, the strong effect of R_{sd} on transistors responses, the quasi uniform effect along the channel (weak local 2D effects). Then using the same approach on short devices with different distances gate edge to STI, we show how to evaluate stress distribution induced by STI as well as its mean value under the gate of the devices. These results help to understand, minimize or optimize stress effects.

1. Introduction

Mechanical stress may be generated in MOS transistors at many technology process steps, as each of them generally implies different process temperature as well as material with different mechanical properties, thermal coefficient mismatch and so on [1]. As CMOS devices continue to be scaled down, these effects become more important. In the case of hetero-structures as SiGe devices, stress is used to improve performances. Otherwise it is mainly detrimental. For back-end part of the process, stress voiding and mechanical weakness of low k materials are of prime importance. For front end part, Shallow Trench Isolation (STI) is today the dominant source of stress in MOSFET channels [2],[3].

Stress induced by STI can in worst case affect yield through dislocations and in consequence the leakage current increases. For lower stress, MOSFETs drivability depends on design layout [4], and each design must be carefully electrically characterized.

While piezoresistivity has been deeply studied in bulk silicon from both theoretical and practical points of view (for sensors), few works have been performed on advanced deep submicron CMOS technologies. Stress is difficult to measure locally and to simulate, since there is a critical lack of data for many thin film materials used in process.

The aim of this paper is to propose a methodology to evaluate the STI induced internal stress in the MOSFETs channel by using a four-point bending method. To reach this goal we present first a piezoresistive analysis of long and short channel nMOS and pMOS of 0.13 µm SOI.

2. Stress induced by STI

Shallow Trench Isolation process may induce significant mechanical stress in devices. Due to a difference in thermal expansion coefficient between silicon and silicon oxide in the STI, visco-elastic effects and side-wall reoxidation during oxidizing thermal anneals, a compressive state of stress develops (Fig. 1).

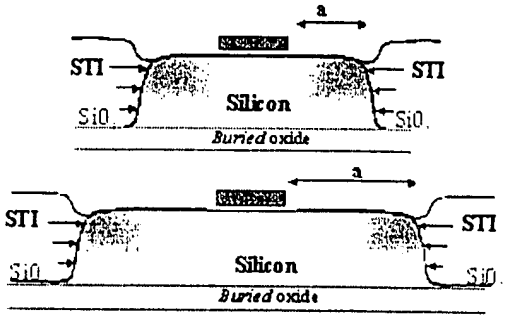

Fig. 1: Schematic of mechanical stress induced by STI.

Through piezoresistive effects this stress modifies transistors electrical parameters, such as mobility. A decrease of nMOS mobility and an increase of pMOS mobility are observed with increasing compressive stress. The higher the distance STI to gate edge is ("a" parameter), the lower the compressive stress is (Fig. 2). The unstressed reference is taken at a=10 µm.

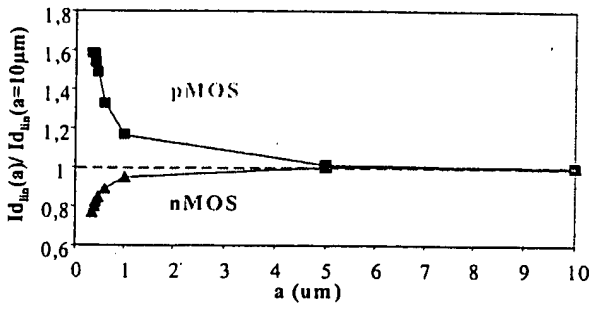

Fig. 2: nMOS and pMOS SOI current versus "a" parameter.

However the relationship is not linear, as the back wafer interface acts as a free surface and tends to impose a zero stress. It has been shown [4] that the typical dependence of the stress versus "a" can be described as:

$$\sigma(a) = \sigma(a_{min})\left[1 + K_\sigma \cdot \left(\frac{a - a_{min}}{a}\right)\right] \qquad (1)$$

where an "a_{min}-MOSFET" is taken as a reference and K_σ is a fitting parameter accounting for stress variations (when $a \rightarrow \infty$) with respect to $\sigma(a_{min})$.

3. Experimental method

A four-point bending technique is used to apply an external mechanical stress on MOSFETs in rectangular strips cut from the wafer. The interest of this method is to have a uniform uniaxial stress between the two central fulcrums if the configuration shown in Fig. 3 is respected.

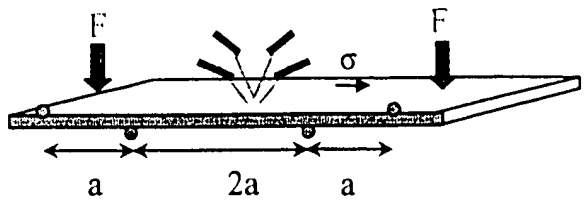

Fig. 3: Four-point-bending method.

The surface stress is calculated from the relationship,

$$\sigma = \frac{12Eyt}{4a^2 - 3L^2} \qquad (2)$$

where E is the Young's Modulus (E=168GPa for (110) silicon orientation), y is the total strip vertical displacement (measured by a micrometer screw), t the total thickness of the strip, L is the length of the strip between the two external fulcrums and a is equal to L/4. The experimental procedure, preparation of samples and calculation errors are described in [5]. The global accuracy is estimated to be around 7%. Stress was limited to 130MPa in order to avoid any sample break. Compressive or tensile stress can be applied. In all cases a continuous linear variation of parameters from compressive to tensile stress was observed. For practical reasons we will refer mainly to one kind of stress. For full piezoresistance analysis, stress was applied in a longitudinal or a transversal direction by appropriate sample preparation.

4. Tested devices

We tested n and p MOS transistors fabricated on (100) silicon substrates for bulk and SOI 0.13µm technologies. Similar results are obtained. We focus on SOI results in this paper.

Studied devices have a gate oxide thickness T_{ox}=2nm, a channel width W=10µm and a long (L=10µm) or short (L=0.13µm) channel length.

5. Experimental results

A. Stress Influence on Long Channel Devices

Figure 4 shows the typical external mechanical stress dependence of nMOS drain current and transconductance Gm characteristics in the linear region of a 10µm long transistor. The mobility variation is the main effect while threshold voltage is unaffected (variation < 3mV for a stress equal to 100MPa), which is consistent with previous results [6].

The variations of $\Delta\mu_0/\mu_0$ versus applied tensile mechanical stress are presented in Fig. 5. An excellent linear dependence was confirmed for both n and p MOS devices. For nMOS technology, the general trend of $\Delta\mu_0/\mu_0$ is to increase (decrease) under tensile (compressive) stress, more pronounced in a longitudinal direction than transversal. On the other hand, for pMOSFETs, $\Delta\mu_0/\mu_0$ decreases (increases) under a longitudinal tensile (compressive) stress and increases (decreases) under a transversal tensile (compressive) stress. These phenomena can be explained by the subband energy level change induced by the external stress in the case of nMOS, added to a band shape modification in the case of pMOS [7].

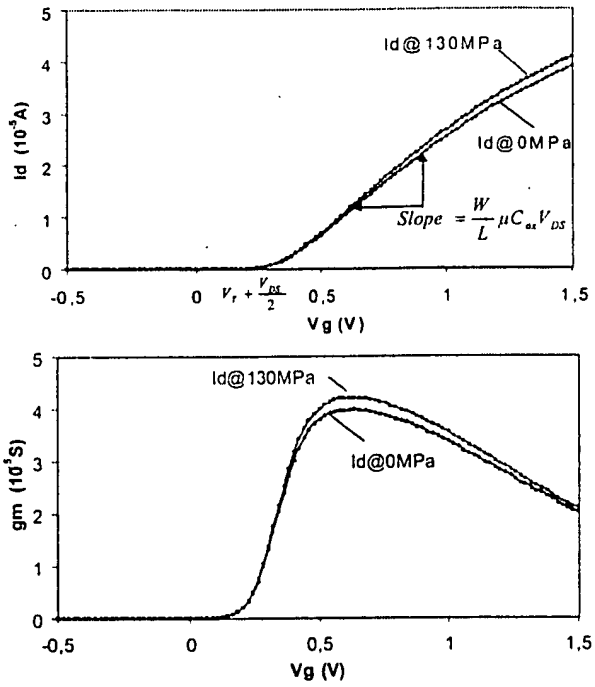

Fig. 4: Linear region transfer characteristics of nMOS SOI for 0 and 130MPa under a longitudinal uniaxial stress.

The mobility variations are related to the piezoresistance response. If we respect the orientation of the device with the crystallographic axes under uniaxial stress, the mobility variations can be reduced to [6]:

$$\left.\frac{\Delta\mu}{\mu}\right|_{0^\circ} = \Pi_L \sigma = \left(\frac{\Pi_S + \Pi_{44}}{2}\right)\sigma \qquad (3)$$

$$\left.\frac{\Delta\mu}{\mu}\right|_{90^\circ} = \Pi_T \sigma = \left(\frac{\Pi_S - \Pi_{44}}{2}\right)\sigma \qquad (4)$$

in which $\Pi_S=\Pi_{11}+\Pi_{12}$, Π_L is the longitudinal coefficient and Π_T is the transversal one. The Π_L and Π_T values are extracted from the slope of $\Delta\mu_0/\mu_0$ versus the applied uniaxial stress respectively from 0° and 90° orientations. Π_{11}, Π_{12} and Π_{44} are the three major coefficients of the cubic structure of silicon.

Table 1 summarizes the piezoresistive coefficients. The signs and magnitudes of these coefficients are similar with those reported in the literature on 0.3µm devices [6]. The observed discrepancies between the data

might be interpreted by the differences in the device parameters such as oxide thickness, substrate doping...

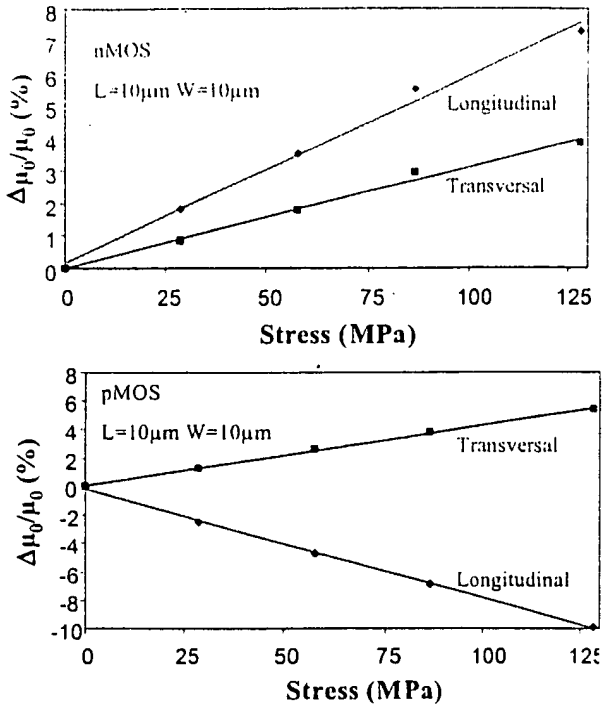

Fig. 5: Normalized mobility change versus applied uniaxial stress.

Table I: Piezoresistance coefficients obtained for the SOI devices (x $10^{-12}Pa^{-1}$). Error estimation: ± $60.10^{-12}Pa^{-1}$.

	NMOS	PMOS
Π_L	580	-767
Π_T	311	422
Π_S	891	-346
Π_{44}	269	-1189

B. Stress Influence on Short Channel Devices

On short channel devices, the source/drain resistance must be taken into account. The influence of the series resistance R_{sd} in linear region is taken into account using:

$$Id = Id_0 \left(\frac{1}{1 - R_{sd} Id_0 / Vd} \right) \qquad (5)$$

Then we calculate the equivalent gate voltage shift to get the same Id with and without the applied stress $\Delta Vg = \Delta Id/Gm = (Id_{unstressed} - Id_{stressed})/Gm$ where Gm is the transconductance. Within a first order differential analysis [8], it can be shown that:

$$\Delta Vg = -\Delta Vt + \frac{Id}{Gm}\left(\Delta\mu_0 / \mu_0\right) \qquad (6)$$

As implied by Eq. (6) a plot of ΔVg versus Id/Gm should give the relative mobility change and the threshold voltage shift, as shown in Fig. 6 for a pMOSFET (note that $\Delta Vt \sim 0$). R_{sd} was extracted using Taur's technique [9], and assumed at first order independent of stress (due to high doping and according to in-house other characterizations and modelisation). For all the devices, even though R_{sd} was low, its impact on the extracted parameter was significant for 0.13µm devices (Fig. 7).

Table II presents an example of calculations including R_{sd} correction in the piezoresistive coefficients for a pMOSFET/SOI with L=0.13µm.

Compared to the long transistor (L=10µm), a quite good agreement is observed for the two experimental coefficients (Π_L, Π_T) and for the major physical coefficient (Π_{44}). The minor physical coefficient Π_S is less precise as the relative extraction error is maximum in this case, Π_S being the difference between two close values.

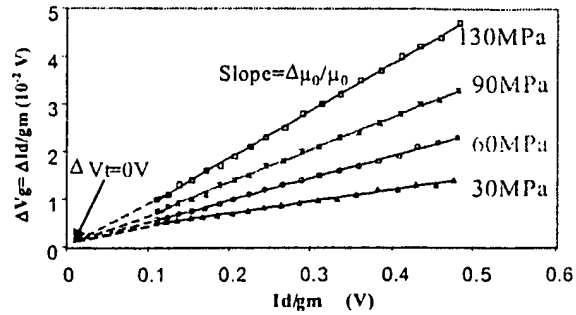

Fig. 6: Variations of the gate voltage shift ΔVg with the quantity Id/Gm after various stress levels for a 0.13µm pMOSFET/SOI.

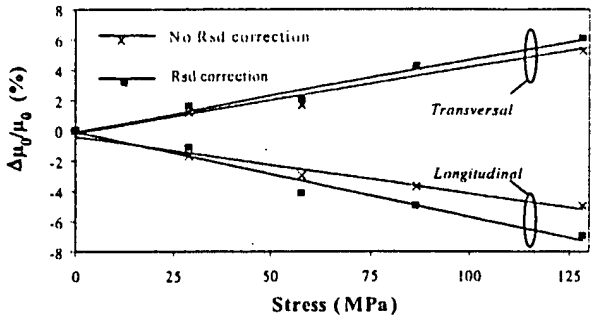

Fig.7 : Normalized mobility change versus applied uniaxial stress as obtained with and without the R_{sd} correction to a 0.13µm pMOSFET/SOI.

Errors in Π_L or Π_T are estimated in the order of ± $100.10^{-12}Pa^{-1}$. Errors in Π_S or Π_{44} are estimated in the order of ± $150.10^{-12}Pa^{-1}$. Consequently the agreement between Π coefficients for both short and long devices remains close to the measurement and extraction errors. An important conclusion to the previous discussion is that local or 2D stress (induced at the gate edge, at junctions, ...) does not affect significantly short devices as compared to longer ones. For this technology, edge effects (gate, junction, ...) may however explain the residual difference between small and long devices.

Table II: Correction Piezoresistance Coefficients for pMOSFET/SOI with L=0.13µm on (100) Silicon (x $10^{-12}Pa^{-1}$).

MOSFET parameters	Measured values	Corrected values	Error
Channel length	0.13 µm		
Parasitic R_{SD}	35 Ω		
V_d	-0.1 V		
Π_L ($.10^{-12}Pa^{-1}$)	**-372**	**-561**	+/- 100
Π_T ($.10^{-12}Pa^{-1}$)	**431**	**469**	+/- 100
Π_S ($.10^{-12}Pa^{-1}$)	59	-92	+/- 150
Π_{44} ($.10^{-12}Pa^{-1}$)	**804**	**-1031**	+/- 150

6. Stress evaluation by bending

Four-point bending method was applied for L=0.13µm transistors with different gate edge / STI "a" distance. For each device a tensile stress from 0 to 100MPa was applied. Data for SOI pMOS device are given in Fig. 8. Two main results are obtained.

First we can observe that for all the devices, the curves Id(σ) are parallel. This indicates that the different sources of stress considered here, namely due to STI and due to bending, are additive. No non-linearity or relaxation effects, etc... are noticed.

Second by exploiting the previous linearity and parallelism, we can extrapolate the curve of "zero stress" transistor, a=10µm, on which external stress is applied, to recover Id value of devices without external applied stress but with STI induced one. This procedure can be considered valid as long as STI induced stress is homogeneous along the channel of the transistor. This is true for these L=0.13µm devices as this length value is considered small, compared with the characteristic 2D behavior of stress which extends to about ~1.3µm.

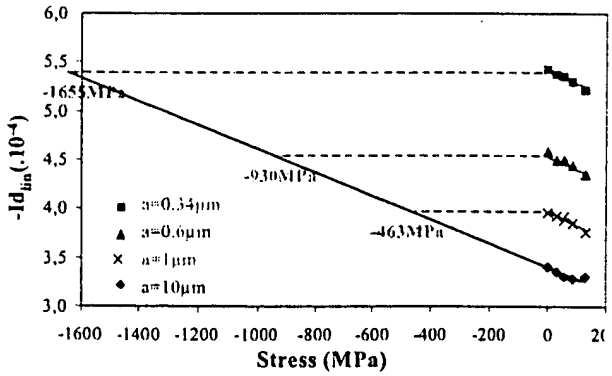

Fig. 8: Four-point bending experiment on pMOS with varying a.

The value of stress in the channels obtained for the different "a" values is shown on Fig. 9. This curve gives a realistic quantitative 2D stress profile versus "a" distance. We observe that stress becomes significant, in this case, at "a"~1µm, in agreement with previous statement. The maximum value obtained for a_{min} is around -1655MPa for pMOS and around -756MPa for nMOS (this difference was clearly visible on Fig. 2).

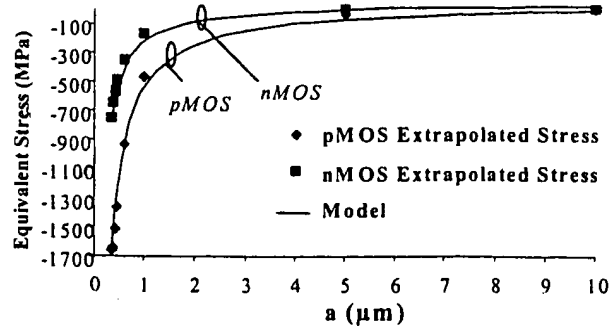

Fig. 9: Stress profile for L=0.13µm devices (experimental results and linear model fitting, performed on nMOS and pMOS SOI transistors).

A very good fit is obtained between the experimental stress profile and the linear model fitting (calculated from eq. (1) with $\sigma(a_{min})$=-1655MPa or -756MPa and K_σ= -1.06 or -1.02 respectively for nMOS or pMOS), for both nMOS and pMOS devices.

7. Optimized process

Previous stress studies helped to understand and optimize stress effects induced by STI. The fabrication of STI was optimized with a new liner process involving low induced stress. An example of reduced stress option versus "a" parameter is given in Fig. 10.

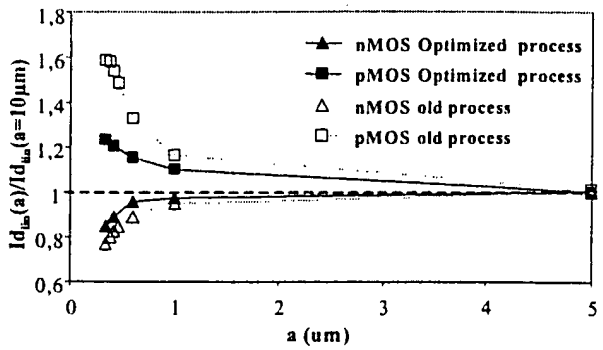

Fig. 10: Id(a) on optimized SOI process.

This new process enables to reduce drastically the effects of STI induced stress on electrical characteristics. For pMOS there is a gain about 40% whereas it is about 15% for nMOS.

8. Conclusion

Using a four-point bending method we have shown that we can get many valuable information on piezoresistance and on stress effects on advanced technologies. We have assessed the stress response on short transistors. We have proved a similar behavior for small and long transistors once R_{sd} effects have been taken into account. To this end, the 2D stress profiles (shape and quantitative values) induced by STI have been extracted and permit to understand and optimize the initial process.

Such methodology and data can have many further applications in the field of simulation calibration, analysis of parameters dependence with stress, analysis of internal stress induced by the process, etc...

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Data Retention Time and Electrical Characteristics of Cell Transistor According to STI Materials in 90 nm DRAM

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Cell transistor and data retention time characteristics were studied in a 90-nm design-rule 512M-bit DRAM for the first time. Also, the characteristics of the cell transistor were investigated for different shallow trench isolation (STI) gap-fill materials. A high-density plasma (HDP) oxide with a high compressive stress increased the threshold voltage of the cell transistor whereas the poly-silazane spin-on-glass (P-SOG) oxide with a small stress decreased the threshold voltage of the cell transistor. The stress between the silicon and the gap-fill oxide material was found to be the major cause of the shift of the cell transistor threshold voltage. When a high stress material was used for STI gap fill, the channel-doping concentration could be reduced, so the cell junction leakage current was decreased and the data retention time was increased.

PACS numbers: 85.30.De, 77.21.Gm, 73.61.Ey, 73.61.Ey
Keywords: STI meterial, STI void, Two-HDP, P-SOG, Cell junction leakage, Data retention time, Threshold voltage

I. INTRODUCTION

As the densities of dynamic random access memories (DRAMs) enter into the giga-bit era, it is essential for the design rule to be scaled down below sub-100 nm [1]. As the design rule shrinks more, the short-channel effect (SCE) increases and various device characteristics, such as the sub-threshold current and the voltage swing, degrade [2]. The most critical issue is the decrease in the threshold voltage and the increase in the sub-threshold current. Therefore, the channel doping concentration should be increased in order to suppress the short-channel effects and to minimize the sub-threshold leakage current. However, high doping levels lead to increased junction leakage currents, which will decrease the retention time.

Recently, data retention times nearly doubled with each successive generation due to the need for high-density, high-speed and low-power DRAMs [3]. The electric field in a memory cell's storage node junction boundary has been becoming stronger, and the leakage current has been increasing with each generation, resulting in poor retention characteristics. The retention time is projected to be an even more serious problem.

Process integration with the design rule of sub-100 nm has many problems. One of the serious problems in the sub-100 nm process is the shallow trench isolation (STI) gap-fill process. Figure 1 shows the variation of the STI aspect ratio with the technology generation. If the STI gap with high aspect ratio is to be filled, a multi-step deposition of a high-density plasma (HDP) oxide or a flowable oxide, such as spin-on-glass (SOG), ozone tetra-ethyl-ortho-silicate (O_3-TEOS) is required. In this study, we used an HDP oxide and a poly-silazane (P)-

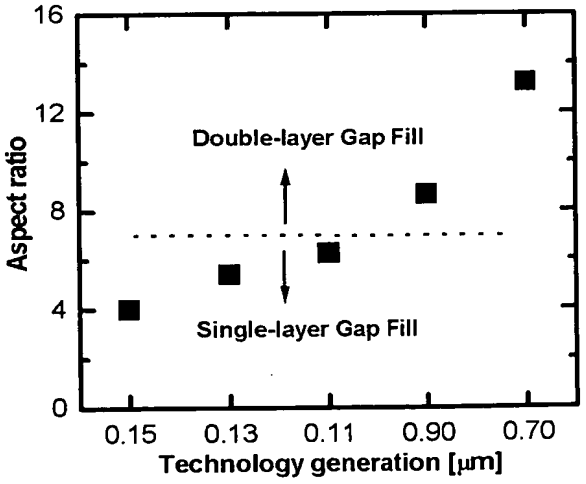

Fig. 1. Variation of the STI gap-fill aspect ratio with the technology generation.

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- Active Patterning
- Trench Etching
- STI Gap-fill Process
- Cell Vth Ion Implantation
- Gate(Poly+WSix) Patterning
- S/D N- ion Implantation
- Gate Spacer & ILD1 Process
- S/D Pad Formation
- BL Formation
- Cap Process

Fig. 2. Major process sequences for fabrication of a DRAM.

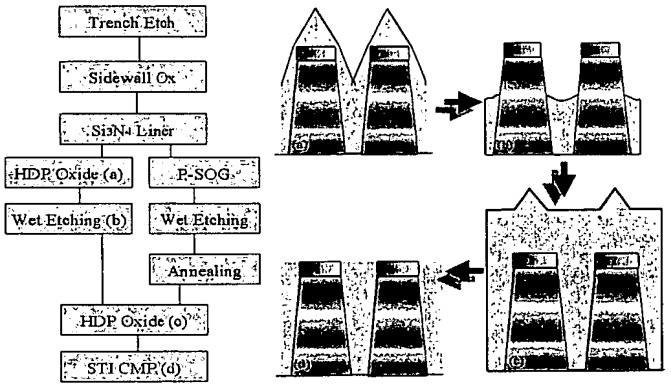

Fig. 3. Process flow for STI gap fill and schematics.

SOG oxide as the gap-fill materials, and we compared their characteristics when used in a cell transistor. The behaviors of the cell transistor's threshold voltage and junction leakage current were studied for different gap-fill materials. The data retention time is also discussed.

II. FABRICATION PROCESS

Figure 2 shows the major process sequence for DRAM fabrication. The process sequence is as follows: First, the active region is defined on the silicon substrate by using photolithography and etching. After trench etching, the sidewall was oxidized and a Si_3N_4 liner was deposited using low-pressure chemical-vapor deposition as shown Fig. 3. Sequentially, a double-oxide-layer process was used to make a void-free STI structure. First, the gap-fill layer was either an HDP oxide or a P-SOG oxide. Then, the proper amount of the first oxide on the active

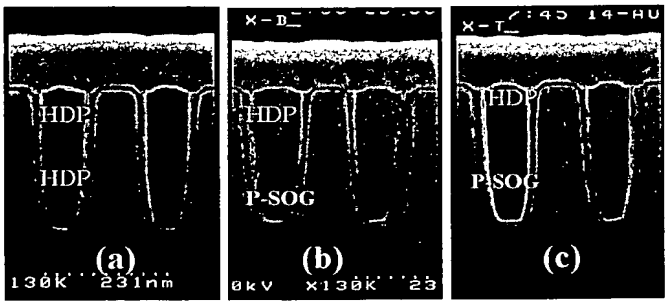

Fig. 4. Vertical SEM photograph of the final STI gap fill process a (a) using double HDP oxide and a (b) and (c) P-SOG+HDP structure.

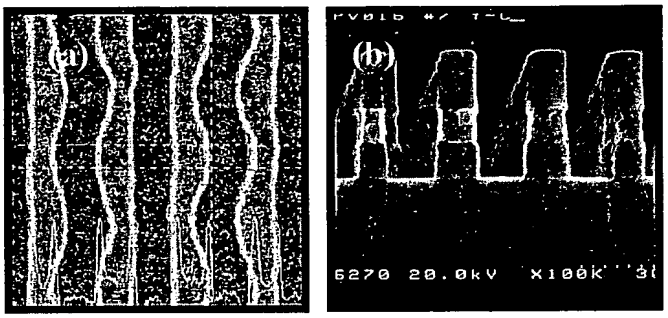

Fig. 5. (a) Top view and (b) vertical SEM photograph after gate etch of the cell array region.

Si_3N_4 mask was chemically removed using wet etching, exposing the over-hang point around Si_3N_4 mask. In the case of the P-SOG oxide as the first oxide layer, a 650 °C wet annealing was added to change the P-SOG layer into stable SiO_2 [4]. Finally, a second HDP oxide layer was deposited, and chemical mechanical polishing (CMP) was used to make a planar surface. Figure 4 shows a cross-section of the STI structure after deposition of the gate poly-silicon. STI with the P-SOG+HDP process shows a clear wet boundary, but STI with the HDP+HDP process does not. To study the effect of the amount of P-SOG oxide gap-fill on the cell transistor's behavior, we split the wet etch time into two parts. After STI process, ion implant processes were executed to form the well and to control the transistor's threshold voltage.

A dual gate oxide process was adopted to cover various performances of various transistors. For gate formation, an 80-nm poly-silicon layer, a 100-nm WSi_x layer, and a 180-nm Si_3N_4 layer were deposited. And then, a photolithography process and an etching process defined the gate patterns. Figure 5 shows a top view and a cross-sectional view of a cell array transistor after gate etching. The gate length of the cell array with a 512M-bit density was about 95 nm. The source/drain extension was formed by implantation. The gate spacer was formed using a Si_3N_4 layer. We deposited an interlayer dielectric (ILD) and used CMP to form a flat surface on the

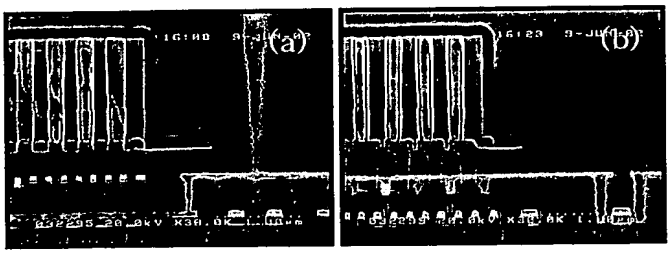

Fig. 6. Cross-sectional SEM photographs of (a) the word-line direction and (b) the bit-line direction in the cell to the core region.

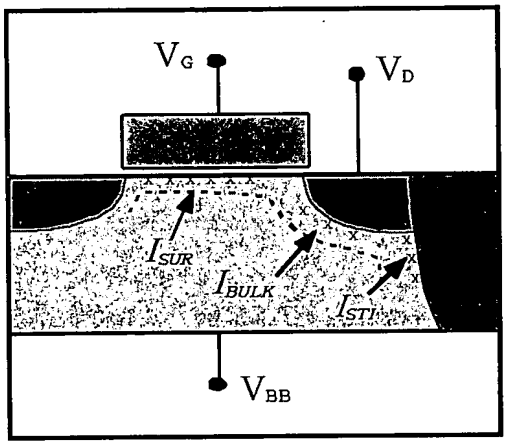

Fig. 7. Schematic cross-section view of the three components in the cell junction leakage current.

ILD in order to provide a sufficient depth of focus (DOF) margin for the photolithography process to come next. The source and the drain regions of the cell transistors were etched by using a self-aligned contact (SAC) etching process, and an N-type dopant was implanted through the SAC openings to reduce the contact resistance. Elevated source and drain contact pads were formed by deposition of doped poly-silicon, and the contact pads were separated by using a CMP process After that, the bit-line process, the cap process, and the metal process were used to complete the DRAM, as shown Fig. 6.

III. RESULTS AND DISCUSSION

The cell junction leakage current is composed of three major components as shown Fig. 7. The first one is the channel-surface-region-induced (*i.e.*, Si-SiO_2 interface) leakage current, I_{SUR}. The second one is the STI sidewall-region leakage current, I_{STI}. The third one is the junction bulk depletion leakage current, I_{BULK}. As the design rule shrinks, the thickness of the gate oxide scales down to compensate for SCE, and the gated-induced drain leakage (GIDL) current increases. The GIDL depends on the gate etch and the re-oxidation

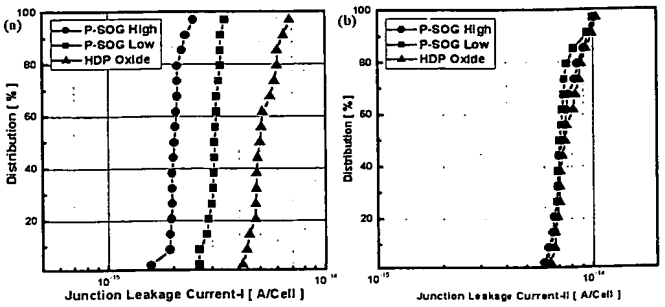

Fig. 8. Comparison of cell (a) DC and (b) BC junction leakage currents for various STI gap-fill materials and P-SOG thickness at the same dose.

conditions. This process-dependent GIDL current has a strong relation to the data retention time [5]. The DC (bit-line contact) junction leakage current, shown in Fig. 8, is the sum of the I_{STI} and the I_{BULK} leakage currents. This DC junction leakage current depends on the first gap-fill material and increases with increasing amount of HDP oxide. The HDP oxide and the P-SOG oxide both have compressive mechanical stress, but the P-SOG oxide has less stress than the HDP oxide because of its lower density. Figure 9 shows the shear stress characteristics when HDP oxide and P-SOG oxide materials are used. The results in Fig. 9 were simulated using TSUPREM4. This lower stress on the bulk silicon reduces the leakage current. As the amount of P-SOG oxide in the STI region is increased, the total stress on the bulk silicon is reduced, and DC junction leakage current is decreased. The BC (storage node contact) junction leakage current, which is shown in Fig. 8, is mostly composed of I_{SUR}. Accordingly, the BC junction leakage current does not change for different STI gap-fill materials. I_{SUR} depends on the electric (E)-field in the BC junction edge, and the E-field depends little on the STI gap-fill material. Figure 10 shows the E-field contour simulation for $V_{ds} = 3.5$ V, $V_{bb} = -0.7$ V, and $V_{gs} = 0$ V. The simulation shows the largest E-field value under the gate edge, and this value increases as the design rule is scaled down. With increasing E-field, the BC junction leakage current increases and the data retention time decreases. For a longer data retention time, the channel and the source/drain junction structure should be optimize as the design rule decreased. This will not be discussed further in this paper.

The threshold voltage of the cell transistor depends on the STI gap-fill materials and the P-SOG oxide volume. If the STI gap is filled only with an HDP oxide, the threshold voltage of the cell transistor is largest. Also the threshold voltage decreases as the amount of P-SOG oxide is increased. If the amount of P-SOG oxide in the STI region is increased, the stress in the bulk silicon decreases. This lower stress in silicon is helpful for enhancing out-diffusion of boron, the channel dopant, during ensuring heat process, such as gate oxidation or re-oxidation. At the same channel ion implant dose, the

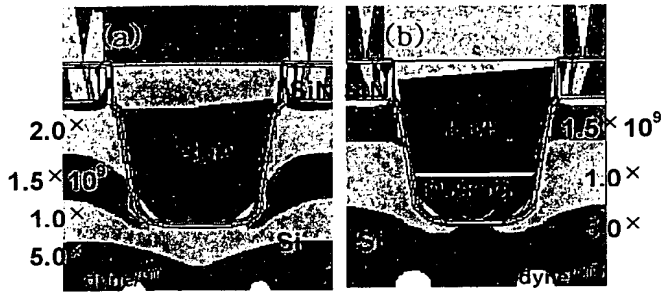

Fig. 9. Simulated shear stress contour of (a) STI HDP and (b) STI HDP+P-SOG.

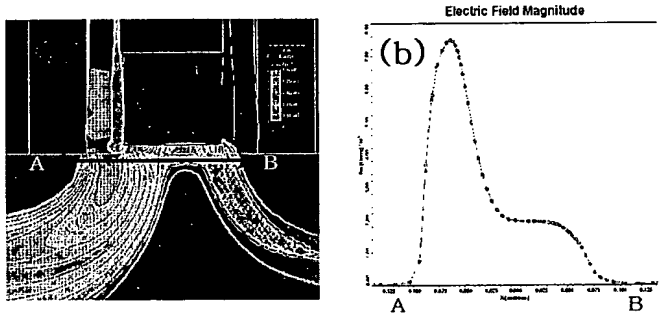

Fig. 10. E-field simulation of a cell transistor with V_{ds} = 3.5 V, $V_{bb} = -0.7$ V and $V_{gs} = 0$ V: (a) E-field contours and (b) cross-sectional view of the E-field magnitude.

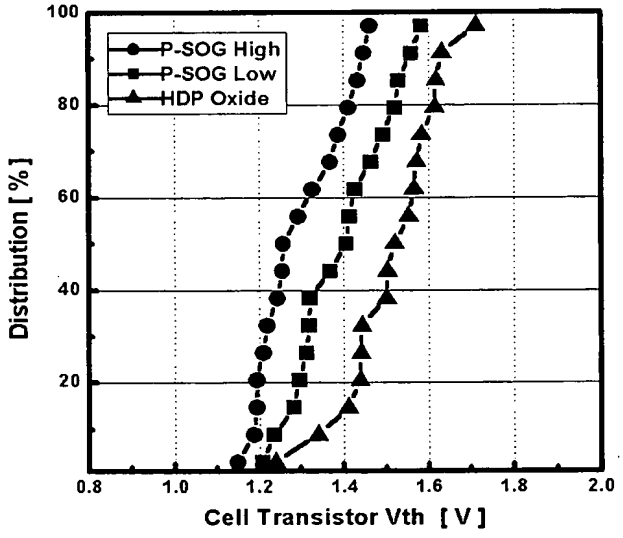

Fig. 11. Comparison of the cell transistor V_{th} for various STI gap-fill materials and P-SOG thickness at the same channel dose.

larger volume of the P-SOG oxide decreases the threshold voltage of the cell transistor. An oxide with a larger stress, such as the HDP oxide, in the STI region will increase the threshold voltage of the cell transistor for same

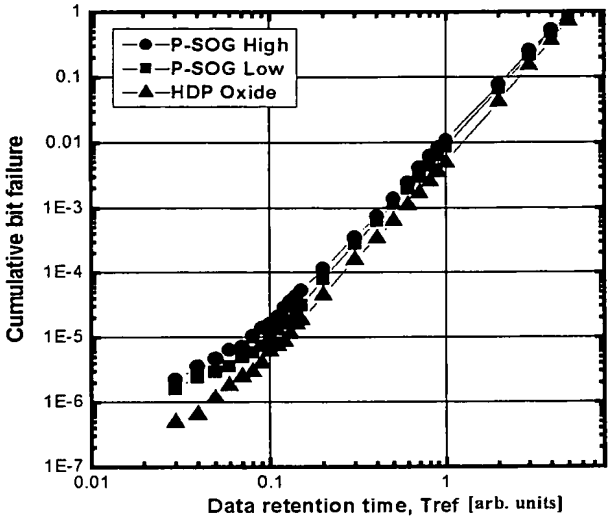

Fig. 12. Date retention curves of samples with different STI gap fill materials and P-SOG thickness at the same cell transistor V_{th}.

ion implantation dose, as shown Fig. 11. Consequently, the channel ion implantation dose can be decreased to achieve the target threshold voltage. Also, a lower channel ion implantation dose will decrease the defect density in the junction boundary of the cell transistor, thereby increasing the data retention time in the DRAM [6]. Figure 12 shows the data retention time for various gap-fill materials at the same cell transistor threshold voltage. Compared with the P-SOG-oxide-filled STI, the HDP-oxide-filled STI needs a smaller channel ion implantation dose to have the same threshold voltage level. Consequently, the cell transistor with the HDP oxide material has a longer data retention time.

IV. CONCLUSION

The data retention time of a 90-nm cell transistor with 512M-bit density DRAM can be improved by using an HDP-oxide gap-fill in the STI region. If the STI region is filled with a larger-stress oxide, the cell transistor threshold voltage is increased, and the channel ion implant dose can be reduced to achieve the target threshold voltage. This lower channel dose will increase the data retention time.

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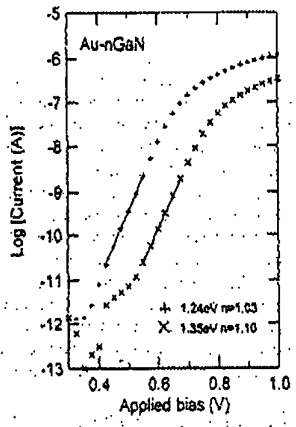

Fig. 3. Forward current characteristics of two diodes, formed on GaN annealed at 600°C, showing the linear region used to extract the Schottky parameters.

good contact uniformity and low tunnelling and recombination currents indicate that these defects are not electrically active for the sample annealed at 600°C. Our TEM results suggest that these states could be related to the Au-GaN interdiffusion region more than to the relatively low density of dislocations observed on the top of the structure. Further work is needed in order to clarify the configuration of this intermediate region. Conversely, after the correlation of structural and electrical characterisations it is evident that annealing up to 900°C to desorb deposited Ga and contaminants following the reflux method has resulted in the formation of electrically active defects at the Au-GaN interface. The formation of a similar complex structure, with the creation of voids and mixed NiO-Au microstructure has been reported on Ni/Au on p-GaN contacts after annealing beyond 600°C (Chen 1999). Other authors have also observed the formation of amorphous regions between (111) TiN crystallites after annealing Al/Ti on GaN (Ruterana 1999). Ohmic contacts are routinely obtained by annealing the metal-semiconductor contact (Kim 1998, Lim 2000). However, in our case the path for the formation of the complex intermixed morphology cannot be attributed to Au diffusion during annealing, since the reflux treatment was carried out before and not after metal deposition. At the moment, we cannot suggest an accurate model for either the morphology or the barrier formation of the samples submitted to Ga-reflux. However, the formation of GaO paths on as-grown defects during Ga deposition (i.e., the first step of the reflux method) may initiate some voids after annealing, so providing sites for Au nucleation and leading to the observed intermixed morphology.

4. CONCLUSIONS

TEM has been used to characterise Au-nGaN semiconductor interfaces formed on GaN surfaces submitted to (i) Ga deposition and re-evaporation at 900°C and (ii) annealing at 600°C. The first method resulted in an intermixed morphology with Au particles embedded in a GaN matrix at the interface region. The second method produced a (111) epitaxial Au layer on GaN. TEM results have provided a possible interpretation of the electrical properties of these interfaces, indicating the origins of the differences between near ideal, high barrier Schottky behaviour for samples annealed at 600°C and low barrier and high ideality factors for samples submitted to the reflux method.

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Strain analysis in sub-micron silicon devices by TEM/CBED

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ABSTRACT: The main aspects of the convergent beam electron diffraction technique (CBED) in a transmission electron microscope (TEM) for the quantitative strain analysis of silicon nanoregions are described. The presently employed procedure to obtain the components of the strain tensor from an experimental CBED pattern is detailed. The method has been applied to the analysis of strain in 0.22 μm active stripes of shallow trench isolation (STI) structures for non volatile memories. The strain distribution along cutlines parallel to the padoxide/Si interface in STI structures with different morphologies can be related to the different technological steps.

1. INTRODUCTION

It is widely accepted that one of the major issues for the deep sub-micron integrated circuit technologies regarding yield, device performance and stability is the mechanical stress built up in the layers and the substrate. It is therefore important to characterise these stresses, which can only be achieved by deployment of reliable techniques for the quantitative determination of these stresses in the substrate with a high spatial resolution. Such work must be combined with dedicated process simulation tools and with sensitive methods to analyse the effects of stress upon device performance.

Presently, the only experimental technique available, which allows one to determine the strain field distribution in sub-micron CMOS devices, without the need of a strain model, is the convergent beam electron diffraction (CBED) technique of transmission electron microscopy. An alternative method based on electron diffraction contrast imaging has also been proposed (Demarest et al 2000). The strain sensitivity of CBED is of the order of 10^{-4} and its spatial resolution is in the nanometer range if a TEM/FEG is employed. In a previous paper (Armigliato et al 1999) we reported the results of this method, as applied to determine the strain distribution along a cutline parallel to the padoxide/Si interface in a 0.80 μm wide recessed-LOCOS (LOCal Oxidation of Silicon) structure. In this paper details are given of the procedure employed to extract the strain tensor from a single CBED pattern taken in a nanoarea of a cross sectioned sample; its application to the quantitative determination of the strain field in 0.22 μm active stripes of shallow trench isolation structures is discussed.

2. EXPERIMENTAL

The TEM/CBED procedure for strain analysis, that will be detailed in the next section, has been applied to shallow trench isolation (STI) structures fabricated by STMicroelectronics (Agrate, Italy)

in the framework of a European project called STREAM (Armigliato et al 2000). These structures are prepared by the following steps. First an isolation stack is grown on the substrate, starting with a thin thermal oxide (10 to 20 nm) and then depositing a layer of silicon nitride by a standard LPCVD (Low Pressure Chemical Vapour Deposition) technique (100 to 200 nm). This stack is successively patterned for the active area definition and for silicon etching by a photolithography process step followed by etching of nitride, oxide and silicon. In this way the silicon trenches are realised, their depth varying from 500 to 250 nm. At this stage, two CVD oxides are deposited to fill the trench. First a layer of a CVD oxide with good gap filling properties, called HDP (High-Density Plasma), is deposited. Then the final thickness is obtained adding either a layer of TEOS (Tetra Ethyl Ortho Silicate) oxide, deposited by LPCVD (see Fig. 1a) or an additional HDP oxide (Fig.1b), deposited with a different sputter etch/deposition rate. The choice of this latter solution results in a better planarisation of the oxide, which can be favourable for the subsequent process steps. After trench filling, the oxides are annealed at a very high temperature to obtain near thermal oxide characteristics. These STI structures are the first step towards the fabrication of 0.15 μm test structures for non volatile memories.

The morphology of these two types of STI structures is shown in the cross sectional images in Fig. 1.

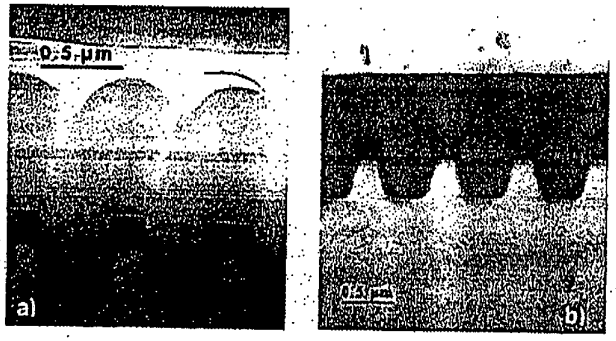

Fig. 1. Comparison between the morphology of the STI structures analysed in this work. The second oxide layer, deposited after trench filling with HDP, is TEOS in (a) and HDP in (b). The different degree of surface planarisation is clearly visible

In the bottom part of these images are visible the silicon active areas, where the TEM/CBED measurements have been taken, and which are delimited by the shallow trenches and the nitride/padoxide overlayers; above the active areas/trenches alternate stripes it is visible the thick second oxide. The planarity of the top surface is quite different in the two cases. The width of the active areas is 0.22 μm and the depth of the trenches is 0.35 μm

The cross sectional TEM samples, obtained by ion beam milling, have been investigated by three different microscopes: (i) a Philips CM30 (LAMEL Institute) equipped with a LaB_6 filament and operating with a 10 nm spot size, (ii) a Jeol 2010F FEG/TEM (University of Sheffield), which features a spot size of 1 nm and is equipped with a Gatan GIF energy filter and (iii) a LEO 922 LaB_6 (STMicroelectronics) equipped with an in-column omega filter. The samples analysed by the Philips and LEO microscopes have been kept at 100 K by a LN_2 cooled specimen holder, whereas in the case of the JEOL microscope room temperature CBED experiments were performed. No energy filtering was available in the CM30 microscope.

The accelerating voltage was 100 kV in <130> zone axis and 200 kV in <230> orientation.

3. STRAIN ANALYSIS BY TEM/CBED

The HOLZ-line method is the most accurate one for local lattice strain measurement. In a fast fully kinematical approach, the extraction of the strain values from the HOLZ-line pattern could be simply performed through a best-fit between computed and experimental patterns. However it is known that HOLZ lines are usually shifted with respect to their kinematical positions due to dynamical interactions of the beam electrons with the crystal potential (a detailed discussion of the dynamical shift has been given by Zuo and Spence (1992)). Accurate results can only be obtained if the simple kinematical approach is modified according to the crystal potential of the zone axis.

In a first order "quasi-kinematical" approximation (Lin et al 1989), dynamical deviations of the positions of HOLZ line are accounted for by using an effective electron acceleration voltage determined from the kinematical best fit of a HOLZ line pattern taken in an unstrained part of the sample. This "quasi-kinematical" correction holds true only if the dynamical interactions between zero order reflections and HOLZ lines and among HOLZ line themselves are not so severe as in low index zone axes like the <111> or <100> in FCC crystal lattices. In these cases dynamical interactions can produce a shift of the HOLZ lines induced by thickness variation of the sample and deviation of the lines from their kinematically expected rectilinear behaviour. Good results on strain measurements based on fast "quasi-kinematical" calculations can then be obtained only if the zone axis is reasonably free from these dynamical effects.

In previously reported experiments on sub-micron LOCOS structures (Armigliato et al. 1999) the CBED patterns were taken in the <130> crystallographic projection, which was shown to be reasonably well fitted using a unique effective voltage correction to the kinematical approach. In order to reach this zone axis, it is necessary to tilt the sample by 26.5° off the <110> direction of the cross-section plane, around an axis parallel to the direction of the crystal growth. This rotation, however, induces a severe projection effect that inevitably worsens the lateral resolution. Then, in order to study strain fields in deep sub micron structures, like the 0.22 μm STI structures analysed in this work, it has been changed the zone axis, where to take the CBED patterns, from <130> to <230>, thus reducing the tilt angle from 26.5° to 11.3°. In parallel, the acceleration voltage has been increased from 100 to 200 kV, to extend the useful range of thickness and to increase the beam intensity. A typical pattern is reported in Fig. 2a.

In order to check the applicability of the effective voltage correction to compensate dynamical interaction on <230> HOLZ lines patterns, dynamical simulations of HOLZ line patterns at 200 keV of unstrained silicon (Fig. 2b) for different thickness (from 150 nm to 240 nm) in the <230> zone axis have been performed, using the EMS programme (Stadelmann 1987). Then a preliminary (beta) version of a software, presently under development by SIS (Soft Imaging System GmbH, Münster, Germany), has been used to perform a skeletonisation of the simulated CBED patterns. Finally, a "quasi-kinematical" fit of these dynamical patterns was obtained for different thickness of the sample, by using the software HOLZFIT (CNR-LAMEL). The best fit was reached using a grid search of the value of the acceleration voltage which minimises the χ^2 function defined by the differences between computed and experimental distances of HOLZ lines crossing points. In Fig. 2c are summarised the results obtained and it is shown that the "quasi-kinematical" best fit is reached with almost the same effective voltage for all the investigated thickness (the overall variation is ±0.02 keV of deviation, which corresponds to a strain uncertainty of 5×10^{-3}). This means that the HOLZ lines positions are almost unaffected by the thickness variation. In addition, assuming an error of 1 pixel in the measurements of the distances, a χ^2 value less than unity is found. This means that the agreement between the "quasi-kinematical" simulated patterns and the dynamical ones is of the order of the measurement accuracy. This indicates that dynamical effects are reasonably small in <230> HOLZ line patterns.

In addition to the unrivalled spatial resolution mentioned in the introduction, the additional superiority of the CBED technique with respect to other experimental methods for the study of the strain field is the possibility to determine the components of the lattice strain tensor from a single pattern. The number of the independent strain components by which a unique solution of the best fit

of a single experimental pattern can be found, depends on the zone axis and on the quality of the pattern itself. In the study of strain distribution in isolation structures, where one dimension along a <110> direction is many orders of magnitude higher than the other one (infinite extension), three components of the strain tensor in the {110} plane perpendicular to the infinite direction are usually used: two diagonal components directed along the <001> surface normal and an in plane <110> direction, respectively, together with an in plane shear strain component. As it is known, a CBED pattern determines the strain tensor of the lattice unit cell that can be easily transformed by a simple rotation into a tensor in the sample reference system.

In order to test the capability of the <230> zone axis to give a unique solution for a three lattice parameter fitting ($a=b$, c, and $\alpha=\pi-\beta$), different strained silicon crystal structures have been dynamically simulated and used as "standards". A unique and accurate solution using a "quasi-kinematical" best fit with three free lattice parameter has been found.

The reduction of independent strain tensor elements from six to three, physically corresponds to both *plane stress* and *plane strain* boundary condition. In fact in the *plane stress* case the angle γ of the unit cell, whose variation is related to the shear strain component ε_{xy}, is linearly dependent from the diagonal components ε_{xx} and ε_{zz}. In the *plane strain* case the angle γ only depends on the ε_{xx} component; then both *plane stress* and *plane strain* conditions allow us to find a unique solution from the best-fit of the <230> HOLZ lines patterns. However, as well known, the *plane stress* condition strictly holds for very small sample thickness (i.e. in the range typically used in HREM experiments), whereas at a beam energy of 200 keV the local sample thickness useful for HOLZ lines analysis is close to 300 nm, if zero-loss energy filtering is used. Therefore it seems reasonable to search for the unique solution according to the *plane strain* condition, thus considering negligible all the lattice displacements on the third dimension, which corresponds to the normal to the TEM cross-section, i.e. to the infinite direction in the bulk structure to be investigated.

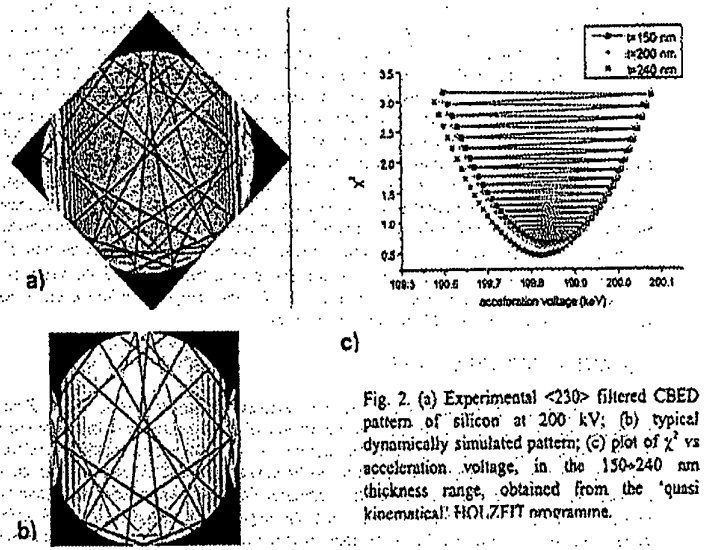

Fig. 2. (a) Experimental <230> filtered CBED pattern of silicon at 200 kV; (b) typical dynamically simulated pattern; (c) plot of χ^2 vs acceleration voltage, in the 150÷240 nm thickness range, obtained from the 'quasi kinematical' HOLZFIT programme.

A self consistent check of the validity of this assumption is at present impossible, as the employed fitting procedure is not so accurate to determine the fourth lattice parameter (γ) in an independent way. Work is in progress in this direction.

4. RESULTS OF THE STRAIN ANALYSIS OF STI STRUCTURES

The procedure outlined in the previous section has been applied to the strain determination in STI structures like those described in Sect. 2. Different trench filling oxidation schemes, nitride thickness and annealing treatments for oxide densification have been investigated. A number of CBED patterns have been taken at 200 kV in a <230> zone axis along a line parallel to the padoxide/substrate interface, in the 0.22 μm active regions of the STI structures. The patterns have been skeletonised by using the above mentioned SIS software, starting with the one taken in an undeformed silicon region (to obtain the effective acceleration voltage). The fit of the computed to the experimental set of distances has been performed through the HOLZFIT programme. A unique solution for the local lattice parameters, and hence the strain tensor components, has been obtained by assuming the plain strain approximation.

In Fig. 3 are reported the plots of the strain distributions along a cutline taken at a depth z=100 nm below the padoxide/substrate interface. Fig. 3a refers to a sample like the one in Fig. 1a, which has a TEOS oxide as the second layer of the STI structure; the three independent components of the strain tensor ($\varepsilon_{xx}=\varepsilon_{yy}$, ε_{zz} and $\varepsilon_{yz}=-\varepsilon_{yz}$) are shown, together with the trace of the tensor ($Tr(\varepsilon)=\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}=2\varepsilon_{xx}+\varepsilon_{zz}$). This last parameter, which represents the local volume variation of the unit cell, has proved to be more useful than the single strain components in the comparison between the CBED values and those computed by a process simulator.

In Fig. 3b are reported the trace tensors yielded by CBED experiments, performed in an STI structure fabricated with a sequence of two HDP oxide films as trench filling steps (Fig. 1b), together with the trace shown in Fig. 3a.

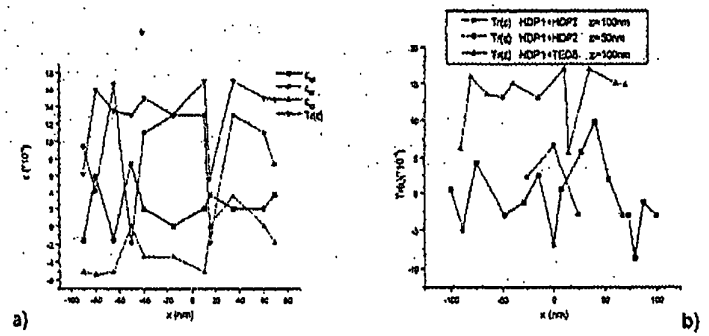

Fig. 3. (a) Plots of strain components and tensor trace along a cutline at z=100 nm for the STI structure shown in Fig. 1a. (b) Tensor trace for both the samples in Fig. 1. A cutline at z=50 nm is also shown.

Together with the results obtained along a cutline at z=100 nm, a few points have been taken also closer to the padoxide/substrate interface (z=50 nm); it is possible in this way to follow the depth distribution of the strain. The reason why the points at z=50 nm are concentrated near the centre of the STI active region is that the increase of the strain gradients close to the edges yields CBED patterns of insufficient quality for an accurate analysis.

It is worth noting that the experimental data reported in Fig. 3 include strain values obtained from both energy filtered CBED patterns, taken at room temperature, and unfiltered patterns, taken at 100 K. The curves show a clear trend, which indicates that the variation with temperature of the dilatation coefficients of the different materials involved (silicon, silicon oxide and nitride) does not affect significantly the strain distribution in the active regions of the STI structure. Although more data is needed to be conclusive, there is strong evidence that CBED analyses at room temperature are feasible. This would be useful for routine applications of the method, as the procedure of sample cooling is time consuming and the cooling sample holders are quite expensive.

From Fig. 3 it comes out that using TEOS for the trench filling generates more tensile strain in the active area, but less compressive strain at its edges, with respect to the case where only HDP oxides are employed. This is a useful information for the choice of the process steps of the CMOS technology.

The strain distribution in these STI structures has been also predicted by the IMPACT process simulator (Baccus et al 2000). It has been found that the use of a pure elastic model for the mechanical behaviour of silicon overestimates the amount of elastic energy in the active area, and a compressive strain is found for the sample in Fig. 3a. However, if the same simulations are performed with an elasto-plastic model, the experimental behaviour of the trace tensors in Fig. 3b is much better reproduced (Senez 2001). This stresses the role of the CBED technique in the improvement of simulation tools, which should become able to suggest process modifications for stress minimisation in sub-micron devices.

6. CONCLUSIONS

In this work it has been demonstrated that the TEM/CBED technique is very useful in the quantitative determination of the strain in sub-quarter micron CMOS technology. The use of TEMs equipped with field emission guns allows one to take CBED patterns with 1 nm electron spots, whereas by energy filtering room temperature measurements can be performed. It is expected that in the near future the procedure to get the strain tensors from a bidimensional array of points in the region of interest of the cross sectioned device will be significantly speeded up, when a software for automatic beam positioning and CBED pattern analysis will be completed. In this way the CBED technique could become routinely employed in the microelectronics industry.

This method is also important in the comparison with the strain field distribution obtained from the simulators of the technological processes; this could allow one to check the validity of the choice of physical parameters and models related to the different process steps.

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Nanoscale characterization of stresses in semiconductor devices

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ABSTRACT: A nanoscale technique for the measurement of stresses has been developed for use in crystalline structures of arbitrary complexity. This has been accomplished by quantitative comparison of transmission electron microscopy (TEM) experimental images with simulations of electron diffraction contrast based upon solutions of the Howie-Whelan equations for finite element method (FEM) generated displacement fields. This procedure allows a quantitative determination of stress fields with nanoscale spatial resolution and ±15 MPa stress sensitivity.

1. INTRODUCTION

As the semiconductor industry continues to decrease the dimensions of microelectronic devices, analytical characterization techniques of high spatial resolution and sensitivity are becoming increasingly important. The principal tool for the ultra-high spatial resolution study of such structures is transmission electron microscopy (TEM). Several electron diffraction techniques exist which can quantitatively measure strains in crystalline materials with a high level of precision. These include convergent beam electron diffraction (CBED) and large angle CBED (LACBED). CBED measurements are performed by examining the displacement of Higher Order Laue Zone lines in electron diffraction patterns. Such measurements are point-by-point in nature and strains as small as 2×10^{-4} can be detected with a spatial resolution on the order of 20 nm (Spence 1992). LACBED can measure strains in a parallel imaging mode, and is capable of determining strain to about 10^{-3} with a spatial resolution of 5-10 nm over areas of about 1.0 μm^2 (Spence 1992). In addition, high strain gradients in the material will compromise the accuracy of these techniques. This paper summarizes a quantitative procedure which utilizes electron diffraction contrast imaging (EDCI) and simulation to obtain a stress sensitivity of ±15 MPa with a spatial resolution of 10 nm over an area of about 1 μm^2—thus examining a volume of material corresponding to that area times the thickness of the sample. Also discussed is the effect of finite element (FE) mesh complexities for properly simulating stresses in focused ion beam (FIB) prepared membranes.

2. QUANTITATIVE PROCEDURE

The quantitative procedure which has been developed comprises several stages. First a FIB machined sample is prepared resulting in an almost parallel sided membrane of known geometry and thickness (measured via standard CBED techniques). A FE model is then constructed of the TEM observed structure in a commercially available software package (ANSYS) incorporating the known cross-sectional geometries and experimentally measured thickness. An artificial temperature load is applied to the FE model to introduce strains into the single crystal material, via use of differential thermal expansion coefficients for the different materials in the structure. An initial approximation of the stresses in the individual materials incorporated in the FE model is provided by wafer curvature measurements of uniform thin films of the corresponding materials. The resulting displacement field information from ANSYS is then used as input for the EDCI simulator: SIMCON

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14.1

Void Free and Low Stress Shallow Trench Isolation Technology using P-SOG for sub 0.1 μm Device

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Abstract

Highly reliable Void Free Shallow Trench Isolation (VF-STI) technology by employing Polysilazane based inorganic Spin-On-Glass (P-SOG) is developed for sub 0.1 μm devices. In order to overcome the difficulties from the gap-filling and accumulated mechanical stress in STI, P-SOG pillar is introduced at the trench bottom. As a result, P-SOG pillar having low stress improves data retention time and hot carrier immunity in 256 Mbit DRAM by reducing cumulative STI stress. In addition, VF-STI shows an excellent extendibility in terms of gap filling capability even at the aspect ratio of more than 10 without void formation.

Introduction

As the design rule of device is scaled down to sub 0.1 μm, the trench isolation technology confronts with serious problems, such as trench gap-filling limitation and involving mechanical stress, which results in device degradation. In the case of STI filled with the conventional High Density Plasma (HDP) oxide, void is formed below 0.11 μm technology node, and mechanical STI stress is increased linearly due to the mismatch with thermal expansion coefficient between HDP oxide and silicon (Fig.1). In the conventional STI, the shallow trench depth for simple gap filling brings additional channel stop implantation, and cell pitch scaling also incur interface state induced by mechanical stress at the STI top corner. These high doping concentration and interface state generation deteriorate data retention time by the increase of GIDL current [1] and hot carrier immunity in DRAM [2]. In this paper, highly reliable VF-STI technology using P-SOG for sub 0.1 μm DRAM is proposed. This technology provides complete gap filling at the aspect ratio of more than 10 and better data retention and hot carrier immunity.

Experimental

Fig. 2 shows schematic diagram of VF-STI. On a pad oxide / Si_3N_4, photoresist was patterned to define active and field region, and trenches were formed. Sidewall oxidation was performed and LPCVD Si_3N_4 liner was deposited to use as an etch stop layer. Then, the trench was filled with 200 nm thick P-SOG (Fig. 2(a)), and etching with dilute HF solution was followed until P-SOG remained at the middle of the trench (Fig. 2(b)). P-SOG was then annealed at 700℃ in an oxidizing ambient. Through this step, P-SOG was transformed to the SiO_2 and became more resistant to the following wet etching. FT-IR spectra of as-spun and after-annealed P-SOG are shown in Fig.3, indicating that P-SOG film was completely transformed to SiO_2. Finally, HDP oxide was deposited to fill the rest of the trench. Then, CMP and Si_3N_4 removal processes were performed (Fig. 2(d)).

Results and discussion

VF-STI technology shows excellent gap filling capability without void formation at 512 Mbit DRAM cell with the isolation spacing of 0.1 μm and aspect ratio of 10:1 (Fig. 4). Comparison of the mechanical stress was performed and stress hystereses of P-SOG and HDP oxide on bare Si are shown in Fig. 5. P-SOG has lower compressive stress than HDP oxide because of its lower density. Fig. 6 and 7 show shear stress characteristics of VF-STI and conventional STI, respectively, which are simulated by TSUPREM4. These results present that the cumulative stress level of VF-STI is lower than that of the conventional STI at the Si/SiO_2 interface.

VF-STI scheme was implemented in fully functional 0.17 μm design ruled 256 Mbit DRAM, and the device performance with VF-STI were found to be comparable to that with the conventional STI.

Fig. 8 shows gate oxide charges to breakdown characteristics measured from rectangular NMOS patterns. No difference is observed between those of VF-STI and the conventional STI, and Q_{bd} values are over 1 C/cm² for each scheme. Fig. 9 shows the transistor I_D-V_G characteristics. Those were evaluated at different substrate-bias voltages to check a presumable grooving at the STI due to chemical attack during the etch back process. There is no difference between VF-STI and the conventional STI. From the previous results, it is concluded that the upper part of VF-STI has almost the same shape as that of the conventional STI. Fig. 10 shows GIDL characteristics measured at various temperatures. GIDL currents of VF-STI are lower than those of the conventional STI at high temperature. It means that the junction leakage current and the band to defect tunneling current of VF-STI are smaller than those of the conventional STI. Also, VF-STI has lower mechanical stress induced leakage current. Fig. 11 shows the I_D degradation in wide and narrow n-MOSFET's after hot carrier stressing. The I_D current degradation in narrow n-MOSFET's owes to interface state generation at the top corner of STI and a narrow width device with VF-STI exhibits smaller drain current degradation. It clearly explains that VF-STI developed less interface state generation than the conventional STI. DRAM data retention curves with VF-STI and the conventional STI are shown in Fig. 12. Fail bits of VF-STI are much smaller than those of the conventional STI. The improvement of retention time is achieved from reduced mechanical stress by employing VF-STI.

Conclusion

Highly manufacturable, low-stress and void free STI process using P-SOG has been developed. Based on the device performance with VF-STI, it can be concluded that this technology is a promising candidate as a future isolation technology beyond 0.1 μm era.

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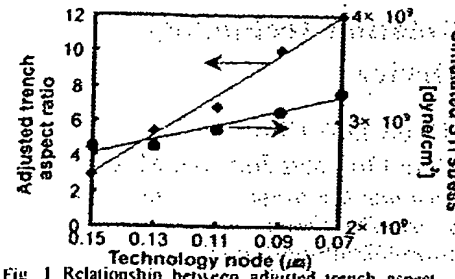

Fig. 1 Relationship between adjusted trench aspect ratio and the highest STI stress according to device scale down.

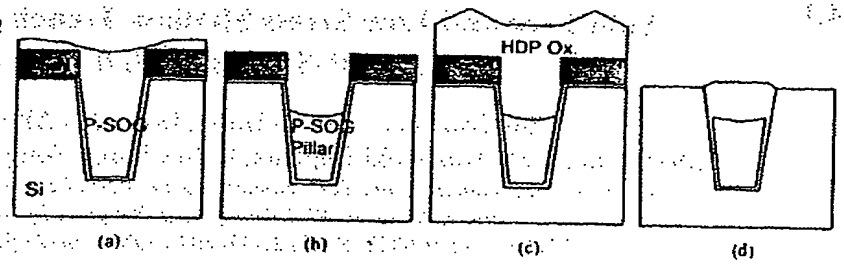

Fig. 2 The schematic diagram of VF-STI : (a) Active definition and P-SOG coating (b) P-SOG etch back and anneal (c) HDP oxide deposition and (d) CMP and SiN strip.

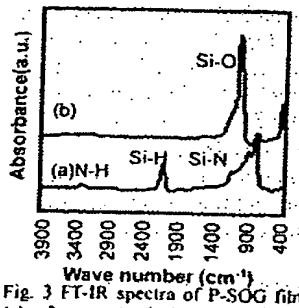

Fig. 3 FT-IR spectra of P-SOG film (a) after coating/soft bake and (b) after anneal under oxidizing ambient at 700℃, 30 min.

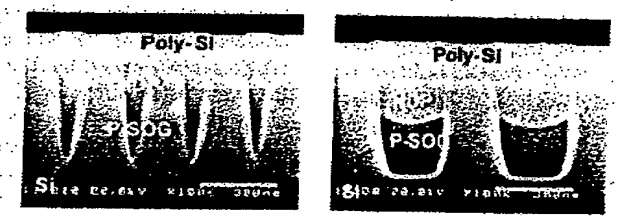

Fig. 4 SEM photographs of the final profiles with VF-STI. Memory cell pitch and aspect ratio are 0.1 μm and 10, respectively. VF-STI shows excellent gap filling capability without void formation.

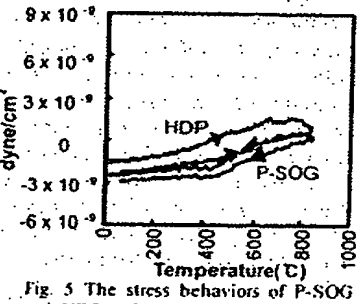

Fig. 5 The stress behaviors of P-SOG and HDP oxide at anneal temperature range. P-SOG has relative low compressive stress to HDP oxide.

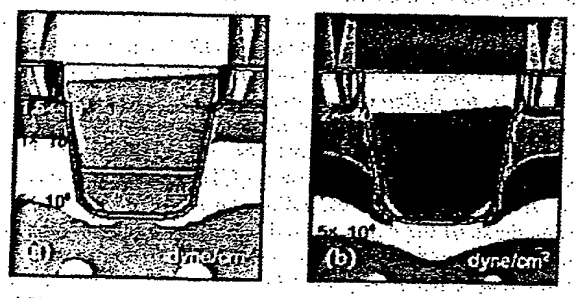

Fig. 6 Simulated shear stress contour of (a) VF-STI and (b) conventional STI.

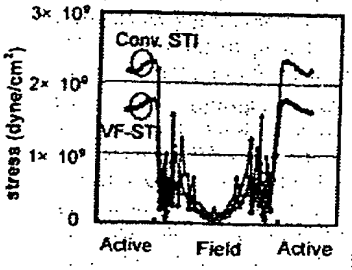

Fig. 7 Comparison of stress along the Si/SiO_2 interface between VF-STI and conventional STI.

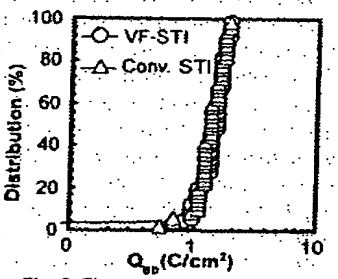

Fig. 8 Charge to breakdown (Q_{BD}) characteristics of n-MOS rectangular pattern.

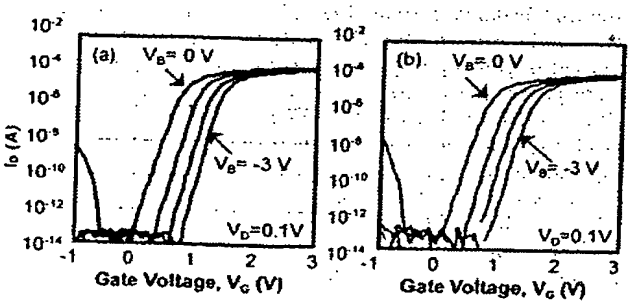

Fig. 9 I_D-V_G characteristics of n-MOSFET's with (a) VF-STI and (b) conventional STI. W=6 μm, L=0.6 μm and T_{ox} = 6 nm.

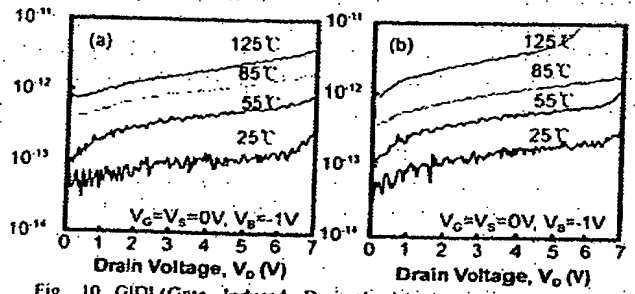

Fig. 10 GIDL(Gate Induced Drain Leakage) measured at various temperatures (a) VF-STI and (b) conventional STI. W=0.23 μm, L=0.17 μm and T_{ox} = 6 nm.

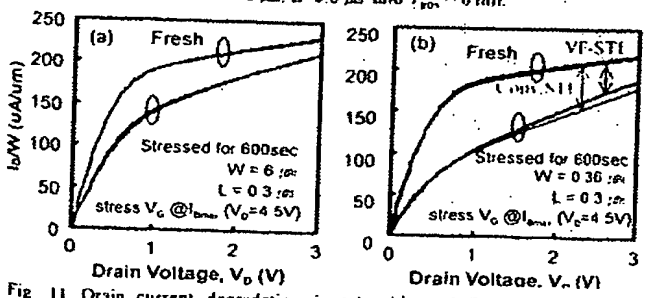

Fig. 11 Drain current degradation in (a) wide and (b) narrow width n-MOSFET's after hot carrier stressing. Narrow width transistor with VF-STI shows less degradation than conventional STI.

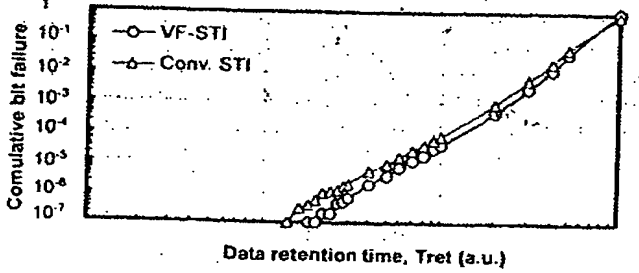

Fig. 12 Data retention curves for the two different isolation scheme. Data retention time of VF-STI is much longer than that of conventional STI.

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Novel Pulse Pressure CVD for Void Free STI Trench TEOS Fill

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Abstract — Because it minimizes the spaces between transistors, the aspect ratio of the shallow trench isolation (STI) become large and it gets difficult to fill STI by conventional LP-CVD TEOS SiO_2 film without void formation. High-density plasma deposition process has been evaluated for better STI fill instead of LP-CVD. But this new equipment costs more than LP-CVD. This paper is to describe a new technique, a pulse pressure chemical vapor deposition (CVD) method for STI fill without forming any voids by using conventional LP-CVD equipment. Pulse pressure enables an uniform source gas supply to the STI trench and a conformal film deposition without void.

INTRODUCTION

The STI process has been used instead of local oxidation of silicon (LOCOS) from around the 0.25-μm feature size generation of LSI. For this STI trench fill, conventional Tetraethoxysilane (TEOS) low pressure chemical vapor deposition (LP-CVD) was used. However as the feature size get smaller, it has become difficult to fill STI trenches without forming any voids. Fig. 1 shows a cross section of a void deposited by the conventional LP-CVD deposition condition (680°C, 1.8Torr), as photographed with a scanning electron microscope (SEM).

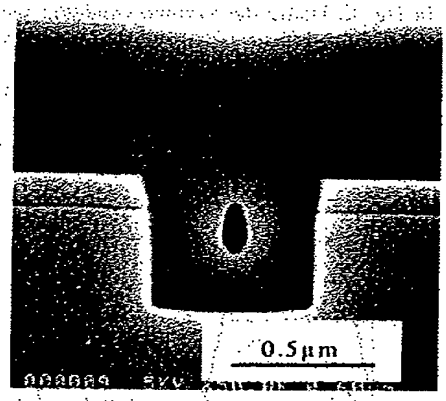

Fig. 1. SEM picture of void cross section as deposited at 680°C

This void will be opened to the air by the following etching processes and induce electrical short of the gate conductors through the etching residual polysilicon in such voids, as shown in Fig. 2.

To solve this void formation, from the 0.18-μm generation LSI, a high-density plasma (HDP) process is being evaluated for void-free films, because of its better film conformality. But silicon oxide (SiO_2) film resistance against wet chemicals etching and film stress view point, LP-CVD TEOS film shows better quality than that of a HDP SiO_2 film as shown in Table 1.

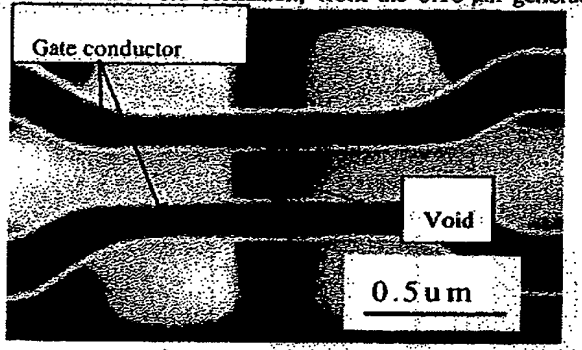

Fig. 2. STI surface picture of gate conductor short through void along the STI pattern

Table 1. Chemical etching rate comparison (before anneal)

	LP- CVD TEOS film	HDP TEOS film
Chemical etching rate (DHF)	1.2 A/sec	7.7 A/sec
ratio	1	6.4

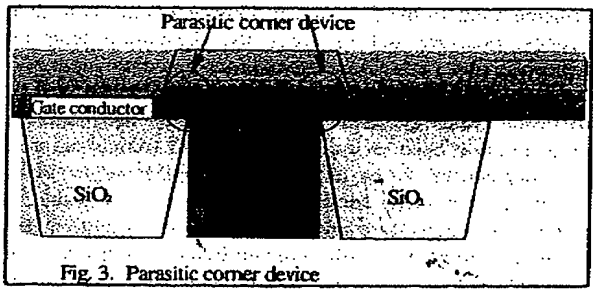

Fig. 3. Parasitic corner device

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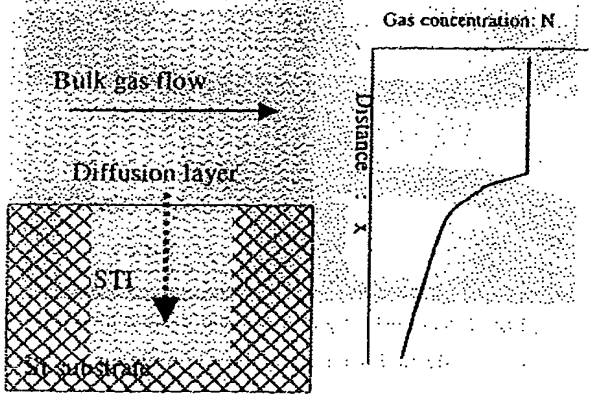
STI SiO_2 film thickness recession induces parasitic corner device as shown in Fig. 3. and degrades sub-threshold voltage device characteristics. Also, the process and equipment cost of conventional LP-CVD is much lower than that of HDP equipment. Therefore it is desired to extend the LP-CVD TEOS oxide use for STI fill below 0.18 μm.

Following is the mechanism of void formation. In the LP-CVD process tube during deposition, the reaction TEOS gas pressure is maintained at a few Torr, and a few micron thick surface diffusion layer exists over the wafers. The TEOS gas diffuses to the bottom of the STI trench as shown in Fig. 4.

This gas diffusion through the surface diffusion layer creates a



$$N(x,t) = N_0 erfc\frac{x}{2\sqrt{Dt}}$$

N : gas concentration
N_0 : bulk gas concentration
x : distance from diffusion layer surface
D : diffusion constant

Fig. 4. Surface diffusion layer over Si wafer and gas concentration in the STI

source gas concentration gradient in the trench (right side of Fig. 4) and leads to non-uniform oxide growth, which causes voids to form. In the diffusion controlled reaction region, gas concentration is described by the equation in Fig.4. Therefore, to avoid void formation, it is necessary to have a uniform gas concentration in the STI trench. One technique is to increase process pressure and to lower the deposition temperature. Lowering process temperature reduces film deposition rate and reaction gas consumption rate. On the other hand, gas diffusion rate is kept constant. With this effect, gas concentration become uniform in the STI trench and uniform film deposition can be expected. The SEM picture in Fig. 5 shows a void cross section deposited at a desirable lower deposition temperature and higher pressure condition (600°C, 4Torr), compared with conventional condition (680°C, 1.8Torr). The void size shrunk but still exists. Further lowering of the deposition temperature is not realistic due to the very long deposition times required.

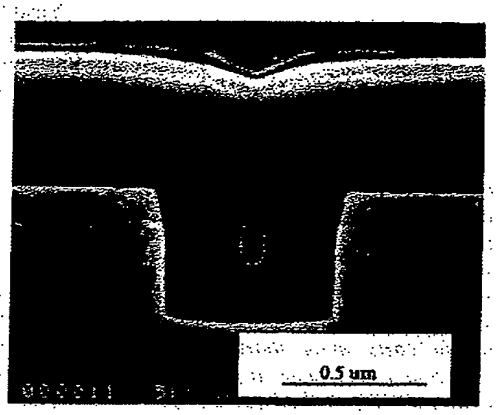


Fig. 5. SEM picture of smaller void deposited at 600°C

To obtain more uniform gas concentration in the STI trench, a "pulse pressure CVD technique" was developed using conventional LP-CVD equipment. This technique uses a modulated process pressure to fill reaction gas in STI.

EXPERIMENT

Pulse pressure LP-CVD STI fill

The new gas pressure diagram used for pulse pressure CVD is shown in Fig. 6. Under the vacuum condition marked (A) in Fig. 6., no surface diffusion layer exists over the wafer. As the gas pressure rises at (B), gas is supplied quickly and pushed into the bottom of the trenches by its own flow, not by diffusion through the diffusion layer. As there is no surface diffusion layer at this stage, a uniform gas concentration in the

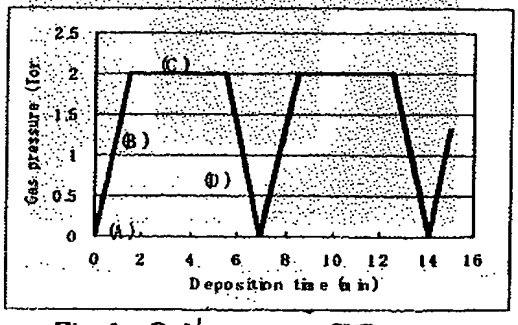


Fig. 6. Pulse pressure CVD pressure diagram

STI trenches can be obtained. Next, the gas flow is held constant for 4 minutes (in this case). At the beginning of the

stable pressure stage (C), due to the gas turbulence, the surface diffusion layer is thin enough so that there is uniform gas concentration in the STI trenches. Before a thick surface diffusion layer is formed, the LP-CVD chamber is evacuated to remove the diffusion layer (D). Because of these effects, a uniform gas concentration in STI trench and a uniform silicon oxide film growth that lead to no void formation are expected. This pressure modulation cycle is repeated to deposit TEOS oxide film to a target thickness. Fig. 7 shows an SEM X-sectional view of a TEOS oxide film deposited by this pulse pressure CVD technique. Process condition of this process is described in table 2.

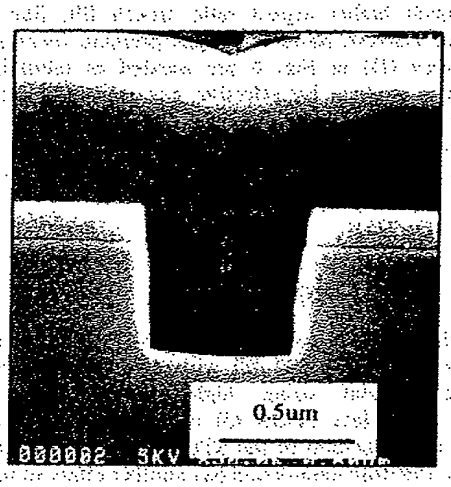


Fig. 7. Void free STI fill using pulse pressure CVD at 700°C, 17 pulse cycles

Table 2. Pulse pressure CVD process condition

Parameter	Condition
Temperature	700 °C
Pressure(High)	2 Torr
Pressure(Low)	10-30 mTorr
TEOS gas flow	200 sccm
Pressure rise period	60-70 sec

This picture shows that trenches can be filled without any voids by using this pulse pressure CVD technique on the conventional LP-CVD equipment.

Film thickness uniformity

TEOS oxide film thickness uniformity within wafer is compared among the films deposited by the conventional LP-CVD and the Pulse pressure CVD in Fig. 8. TEOS film thickness uniformity of the wafer located at the top and bottom of the boat shows a convex and concave shape, respectively. This thickness uniformity tendency is same as that of the conventional CVD. Thickness uniformity trend within CVD tube is shown in Fig. 9. Thickness uniformity at the top portion of the boat(36-85 wafer slot) is worse than that of conventional CVD.

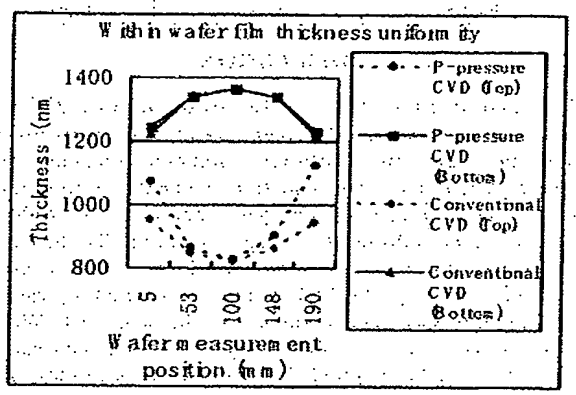


Fig.8 Within wafer thickness uniformity comparison

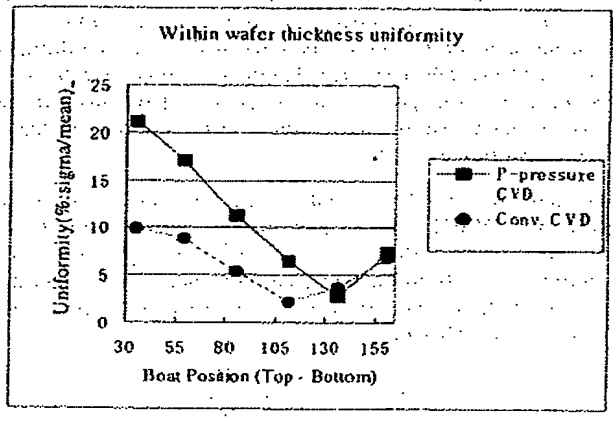


Fig.9 Within wafer uniformity by wafer position

Gas consumption efficiency

As pulse pressure CVD process includes rapid pump down sequence, source TEOS gas loss during pump down is a concern. Table 3 shows a source TEOS gas consumption efficiency. Gas consumption effiçiency is calculated by using the value of the TEOS oxide film thickness divided by total TEOS gas supplied to the LP-CVD tube. Source TEOS gas is deposited on the wafer more effectively by 26% when pulse pressure CVD technique is applied.

Table 3. TEOS gas consumption efficiency

	Pulse pressure CVD	Conventional CVD
Gas consumption efficiency	57.6 nm/L	45.7 nm/L
Ratio	1.26	1.00

DISCUSSION

Conventional LP-CVD uses the diffusion limited reaction region to achieve good within wafer and wafer-to-wafer uniformity. But this diffusion limitation reaction region induces reaction gas concentration gradient. As film growth rate is proportional to the gas concentration, with this condition, non-uniform film is deposited in the STI trench that lead to void formation. Pulse pressure CVD technique enables to supply source gas to the bottom of STI trench by gas flow and uniform gas concentration can be achieved. Without diffusion layer that is mandatory factor for conventional LP-CVD to achieve good film thickness uniformity, pulse pressure CVD could demonstrate equivalent film thickness uniformity at the lower half portion of the boat. The reason of the bad uniformity of the film thickness at the top portion of the boat is thought as follows. Due to the TEOS gas flow rate limitation of the tool during pressure ramp up, TEOS gas is consumed at the bottom of the boat as there are no diffusion layer and enough unreacted TEOS gas cannot reach to the wafer at the top portion of the boat to have uniform gas concentration. To improve within wafer uniformity, higher source gas flow is needed.

In conventional LP-CVD tube, some amount of source gas does not contribute to film deposition because of the existence of the surface diffusion layer. As pulse pressure CVD minimize this diffusion layer, the percentage of the gas that reaches to the growing film surface increase and improves gas consumption efficiency.

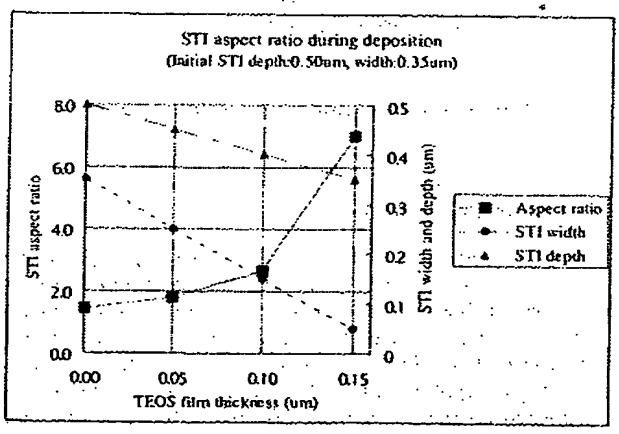


Fig. 10 Dynamic changes of surface aspect ration during film deposition

For the higher aspect ratio STI than this experiment sample, voidless TEOS film fill capability is examined by using Fig. 7 and Fig. 10. During TEOS deposition, STI aspect ratio increase as TEOS film thickness increase as shown in Fig. 10. For example, when 0.15um thickness TEOS deposited on STI with 0.35μm width and 0.50μm depth, STI aspect ratio reaches 7 (STI widhth:0.05μm, depth:0.35μm). Pulse pressure CVD process can fill STI with this high aspect ratio without void formation as shown in Fig. 7. This means that pulse pressure CVD has a capability to fill TEOS without void beyond 0.18μm LSI generation.

For the much higher aspect ratio trench fill, like trench capacitor of DRAM, more rapid gas pressure increases (B) and decreases (D) in Fig. 6 are needed to minimize gas concentration gradient by effective gas pushing in trenches This ideal condition would require a modification of the LP-CVD equipment. For example, equipping it with a source gas supply reserve tank for quick gas supply and a vacuum buffer tank for fast gas pressure down.

CONCLUSION

We have shown that a pulse pressure CVD technique is very effective for void free STI fill with conventional LP-CVD equipments without using high-density plasma CVD equipment. Void less TEOS fill is achieved by supplying source gas to the bottom of the STI trench with gas pressure modulation. Pressure modulation has another effect to improve gas consumption efficiency by 26% because of the minimization of surface diffusion layer thickness.

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Defect Control of STI Process Technology

By Kensuke OKONOGI,* Kousuke MIYOSHI† and Akio TODA‡

ABSTRACT Shallow Trench Isolation (STI) is indispensable for achieving high-density devices. One of the most severe problems with STI is that dislocation generation causes abnormal leakage current. We evaluated the defect behaviors of different STI processes. Dislocation is caused by localized stress near a trench. To clarify the generation mechanism, the relationship between dislocation density and strain near trenches was investigated. These results show that narrow trenches with steep profiles generate the dislocations. It is also realized that dislocation is caused by localized strain at the bottom corners of the trench. Thus, the trench structure needs to be optimized to reduce the dislocation and leakage current.

KEYWORDS **Shallow Trench Isolation (STI), Defect, Dislocation, Oxidation-induced Stacking Fault (OSF), Junction leakage current, Stress and strain**

1. INTRODUCTION

STI (Shallow Trench Isolation) is an isolation technology that is indispensable for achieving higher packing density devices, as the isolation pitch is scaled down for the future devices. One of the most severe problems with STI is the dislocation generated during the device fabrication, which cause abnormal leakage current and chip failure during the loose function test[1]. Therefore, the defect control technology is extremely important when using STI to develop highly reliable devices.

There have been many reports on dislocations near trenches. Dislocations were observed after source/drain implantation[2,3]. However, the defects, which are generated by deep ion implantation during STI process, have not yet been investigated. Therefore, it is necessary to clarify what types of defects are generated by well implantation during STI process. On the other hand, although it is believed that dislocation is caused by localized stress near trench, there have been no systematically studies on the relationship between the localized stress and dislocation density for various STI processes. Thus, it is important to measure the stress distribution near the STI and understand the mechanism of the localized stress in order to eliminate the dislocations.

In this report, the behavior of the defects caused by deep ion implantation for various STI processes was examined. In particular, the strain profiles along the active/isolation interface were measured for several STI structures and the correlation between strain profile and dislocation density was investigated.

2. EXPERIMENT

2.1 Experimental Procedure

The ion implantation forms the nuclei that generates the defects. Many defects are generated by a combination of ion implantation damage and STI stress. Therefore, the defects generated during two opposing processes were observed by using the SECCO etching method. In one process, the ions were implanted after forming the trench (process-A). In the other process, the trenches were formed after implantation (process-B). The defect density and junction leakage current for both processes were investigated. High-temperature annealing after implantation has been generally used to eliminate the damage induced by ion implantation. Two different annealed samples were thus prepared to investigate how the annealing temperature affects the defect density and leakage current for process-B.

Mechanical stress would generate dislocation near the interface between STI and active layer. Also, different trench structures have different types of mechanical stress. Therefore, we investigated how the STI structure (i.e., sidewall taper angle and isolation width) affects dislocation density for process-A. The relationship between dislocation density and strain near the trench was evaluated to clarify the mechanism that generates the dislocations. The SECCO etching method was applied to determine the dislocation density. In order to measure the accurate strain distribution near STI, convergent-beam electron diffraction (CBED) method[4] was used for the strain distribution measurements of the two trench isolation pitches.

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2.2 STI Process Flow

Figure 1 shows the basic STI process flow in this study. After Si_3N_4/SiO_2 deposition, the active areas were defined by the stack layers, and the isolation area was then etched. The etched silicon surface was cleaned to remove the contamination and deposition during trench etching. The trench sidewall surface was oxidized to a thickness of 20nm and HDP-CVD oxide was deposited to fill the trench. Photo resist was applied to etch back the oxide and stopped on the Si_3N_4 mask, global planarization was achieved using the CMP process. The Si_3N_4 and oxide were removed in a wet solution after annealing for the densification of filled oxide was carried out. Through-oxide was formed for the ion implantation, and the gate oxide was formed after removing the through-oxide. In process-A, boron ions for well formation were implanted after the through-oxide was formed. In process-B, boron ions for well formation were implanted before Si_3N_4 deposition is carried out. Annealing was carried out in N_2 atmosphere at 750 or 1,100°C to eliminate the damage caused by ion implantation. Boron ions were implanted at 300keV with doses ranging from $2 \times 10^{13} \sim 5 \times 10^{13} cm^{-2}$.

3. RESULTS AND DISCUSSIONS

3.1 Defects

Figure 2 shows the SECCO etched samples for processes-A and -B at the wide isolation area. Oxidation-induced stacking faults (OSFs) were observed only on process-B samples. The OSF density depends on both the boron dose and the annealing temperature after boron implantation (Fig. 3). The high-temperature annealing effectively removes the implantation damage. Therefore, OSF density of high-temperature annealed sample was reduced.

Figure 4 shows the junction leakage current for process-A and -B samples. Abnormal leakage current was observed only on process-B samples. The OSF of these samples causes abnormal leakage current. In process-B, the trench surfaces were damaged by trench etching and implantation was directly oxidized. These damages behave as the nuclei for the generation of OSF. Therefore, the growth of these nuclei can generate OSF during the sidewall oxidation. However, in process-A, implantation damage does not occur before sidewall oxidation. Accordingly, OSF is not easily generated since the surface before oxidation has a lower nucleus density. We believe

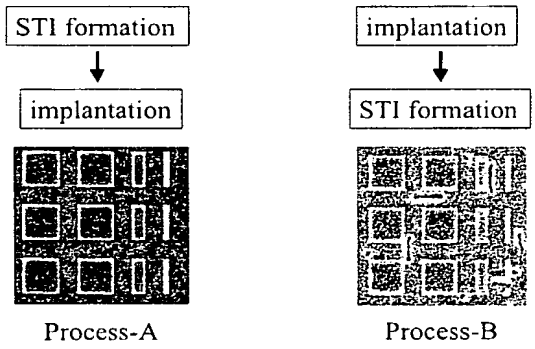


Fig. 2 SECCO etched sample for two different processes at wide isolation width.

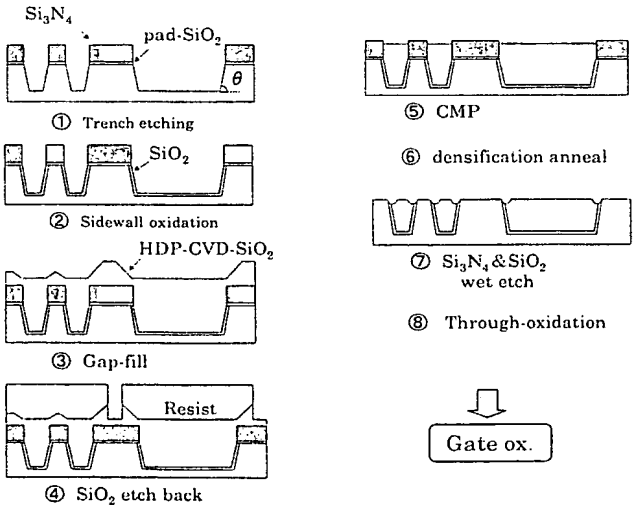


Fig. 1 STI process flow.

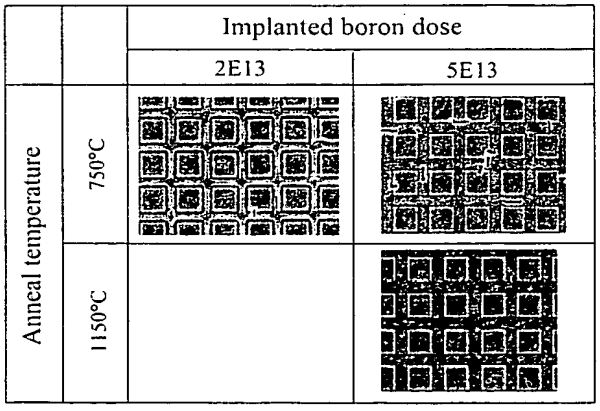


Fig. 3 OSF density dependency on boron dose and annealing temperature.

that etching damage does not generate the OSF nucleus but with the implantation.

Photo 1 shows the SECCO etched samples for both processes at the narrow isolation area. Dislocation is only observed on the process-A sample at the narrow isolation width. Our investigation of process-A shows that dislocation generates after the gate oxidation following ion implantation.

These results indicate that the dislocation will not be generated by the STI stress alone. The damages from the ion implantation in the strained silicon near the trench are one of the major causes for the generation of dislocation. In the next experiment, the dislocation behavior in process-A for several trench structures was investigated.

3.2 Dislocation Behavior

Figure 5 shows samples of 90- and 80-degree sloped trenches after SECCO etching. Trench dislocations were observed only on the vertical trench sample. The junction leakage current increases with the increasing of the slope angle of the trench sidewall. Figure 6 shows the relationship between the junction leakage current and the isolation width. The magnitude and variation of the junction leakage current increases with the decreasing of the isolation width. The narrower the isolation width is, the higher the abnormal leakage current will be.

In order to determine where the dislocations generate and what causes them, we examined the dislocations near the trench by using cross-sectional TEM and measured the strain profiles near trench for two samples with different isolation widths using the CBED method.

Photo 2 shows a cross-sectional TEM image of the trench. All the dislocations were found to occur at the bottom corner. Figures 7(a) and 8(a) show the normal strain components (ε_{XX},ε_{YY}) and shear strain component (ε_{XY}) measured along trench profile for 0.2 or 1.0μm wide trenches. None of the strain

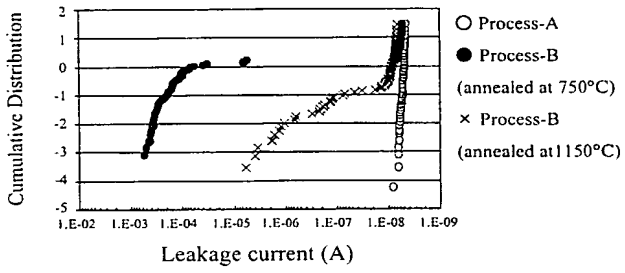


Fig. 4 Junction leakage current for two different STI process.

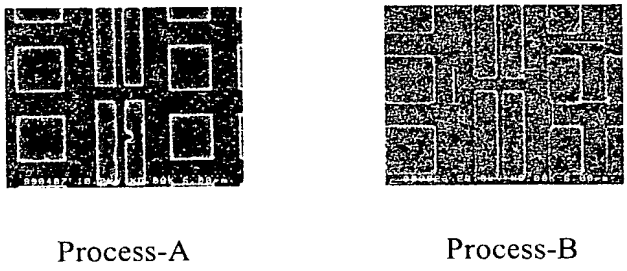


Photo 1 SECCO etched sample for different processes at narrow isolation width.

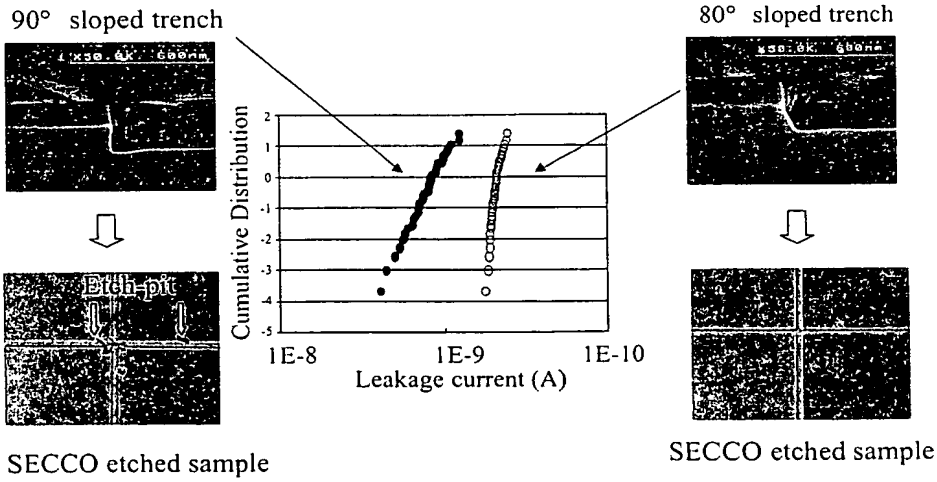


Fig. 5 Slope of trench sidewall dependence on leakage current and dislocation.

measurement samples were ion implanted or annealed in order to avoid the release of the residual strain after the dislocation was generated. Figures 7(b) and 8(b) show cross-sectional TEM images of the measured positions around the trenches. The x- and y-axis are along the horizontal and vertical directions, respectively. In Figs. 7(a) and 8(a), ε_{XX} at the bottom of the trench and ε_{YY} at the sidewall had positive values (tensile strain). This tensile strain at the SiO_2/Si interface is attributed to the difference in the thermal expansion coefficients of silicon and silicon oxide. Localized strain peaks in ε_{XX} were observed at the bottom and top corner for both samples. In particular, the strain peak at the bottom corner was

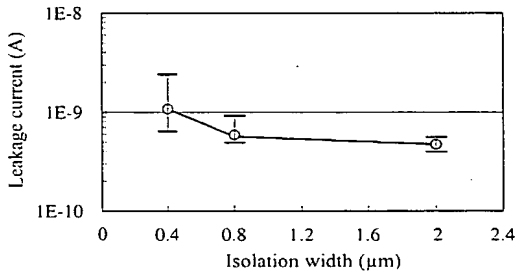
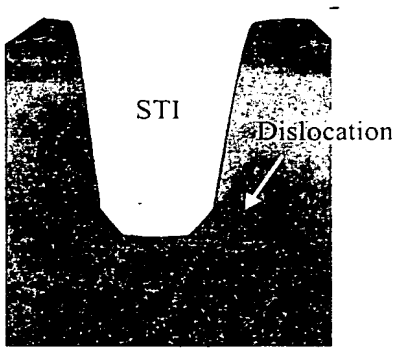
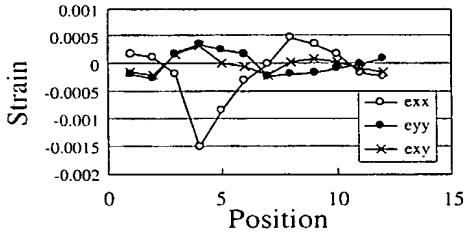


Fig. 6 Isolation width dependence on leakage current.

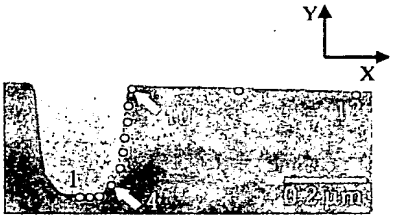


X-TEM image

Photo 2 Generated dislocation at the bottom corner of trench.

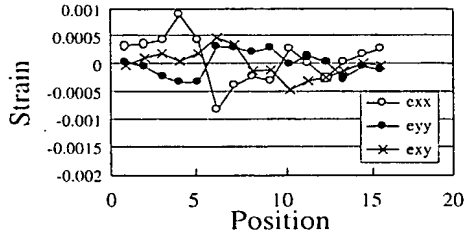


(a) Three profiles of strain components around trench.

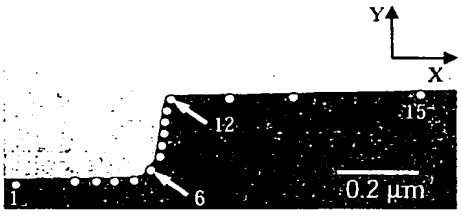


(b) Cross sectional TEM image of strain measured positions.

Fig. 7 Silicon strain measurement around the STI with 0.2μm width using CBED method.



(a) Three profiles of strain components around trench.



(b) Cross sectional TEM image of strain measured positions.

Fig. 8 Silicon strain measurement around the STI with 1.0μm width using CBED method.

the strongest for both samples. Furthermore, the value of the peak at the bottom corner was stronger for the narrower trench. The strongest peak was located at the site where the dislocation was generated. These results indicate that dislocation is caused by localized strain at the bottom corners.

The results of the strain measurement and SECCO etch-pit observation showed that dislocation is more easily generated for samples with the narrower trench and steeper profiles, since these types of trenches suffer the greater amount of stress. Additionally, we found that dislocation is caused by the localized strain at the bottom corners of trench. Therefore, the trench structure needs to be optimized to reduce the dislocation density and the leakage current.

4. CONCLUSION

The defect behaviors for different shallow trench isolation processes were investigated. It is realized that boron implantation used for well formation caused oxidation-induced stacking faults and dislocations. Dislocation is generated when ion implantation damage is induced in the strained silicon near the trench, but not when only STI stress exists. Additionally, the dislocation is generated more easily in narrower trenches with steeper profiles. The stress is strongly depends on trench width and profile. An optimized STI structure can thus reduce the dislocation density and the leakage current.

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Mr. Toda is a member of the Japan Society of Applied Physics, the Physical Society of Japan, and the Japanese Society of Electron Microscopy.

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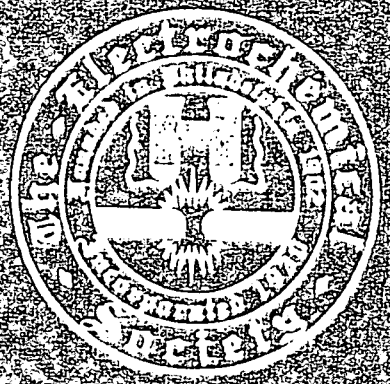
ULSI PROCESS INTEGRATION



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CRITICAL STATES OF STRESS EVOLUTION IN SILICON STRUCTURES OF ULSI WITH SHALLOW TRENCH ISOLATION

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Stress-induced defects in silicon device structures with shallow trench isolation have been studied using preferential etching technique and transmission electron microscopy. First dislocations occurred during trench filling, their density increased throughout the device fabrication process. Dislocations were found to nucleate at the trench side-walls. This enabled using 2-dimensional stress simulations in the search for the STI processing steps responsible for defect generation. Mechanical characteristics of CVD gap-fill oxide were experimentally measured for the calibration of the simulation models chosen. Vulnerability of STI structures to stress-induced defects at different characteristic processing stages was estimated using the results of stress evolution modeling. It was discovered that critical stress states are realized during gap-fill oxide annealing. The intensity of stresses after this stage is the highest and does not change significantly during the subsequent processes. The deeper stress relaxation in as-deposited gap-fill oxide is achieved during its annealing, the more vulnerable STI structures become to dislocations.

INTRODUCTION

Since 80's Shallow Trench Isolation (STI) had been considered as a potential alternative for traditional LOCOS isolation in CMOS device fabrication. Yet only lately, with the industry continuing drive towards the further product miniaturization, costly utilization of complex STI schemes is being justified and they are becoming the dominating or even sole option for sub-quarter-micron CMOS technology generations. Recent advances in such fields as Chemical-Mechanical Polishing (CMP) and Chemical Vacuum Deposition (CVD) of void-free gap-fill dielectrics provide successful implementation of STI. However, there are still some fundamental issues to be solved.

The concern regarding stress-related problems in STI processing was expressed long before this technology entered the field of commercial manufacturing. Analyzing the stress field in model silicon structures with parallelepipedic trenches, S. M. Hu came to a conclusion that the stress might exceed the critical resolved shear stress for dislocation propagation in silicon (1). The increasing number of reports on dislocation observed in STI structures has proved that stress-induced defects are one of the major issues of STI technology (2).

CVD oxides used in STI as gap-fill dielectric material are supposed to be annealed aiming the oxide structure densification and reduction of its etch rate during the following processing steps. The oxidation of trench side-walls during the post-deposition annealing of gap-fill oxide in oxidizing ambient was assumed by H. S. Lee et al. to exert the extreme stress towards the active device areas causing dislocation generation (3). The

annealing in nitrogen was consequently recommended for defect prevention. K. Ishimaru et al. compared defect densities in STI device elements having gate electrodes of different sizes (4). They decided that STI defect generation is controlled by the combined mechanical stress related to gap-fill oxide and gate material. They also found that gap-fill oxide annealing at temperatures as high as 1200°C provided defect-free STI structures. J. Damiano et al. did not find any significant impact of stress in gate stack on the incidence of dislocations (5). In their work, the annealing at higher temperatures resulted in lower defect density as well. However, it was concluded that stress reduction alone can not prevent the formation of STI-related dislocations. The elimination of MOSFET Source/Drain implantation-induced defects was regarded as a key for defect removing in STI structures.

The differences between these conclusions arose probably because they represent rather the case studies of particular processes, materials and geometry of STI structures. Additionally, experimental study of defect density vs. process conditions does not distinguish the effects of dislocation nucleation and their propagation. This might cause the confusion in the interpretation of the results.

The objective of the present work was to unveil the development mechanism of the driving force for dislocation generation in silicon structures with STI. This was considered as a prerequisite for predicting the optimum material properties and process conditions for obtaining defect-free technology. It occurred to the authors that the study of stress evolution in STI processing was the best way for identification the technology steps critical in terms of both defect nucleation and propagation. Stress modeling approach was chosen and extensive experimental investigations of defect distributions in STI structures were needed to apply simulation models correctly. For calibration of the utilized simulation tool, experimental measurements of thermomechanical properties of the materials involved in STI processing were also required.

EXPERIMENTAL

Device structures were fabricated on CZ (100) 200 mm p-type boron-doped silicon wafers with a resistivity of 6 - 9 Ohm·cm. The hard mask stack of thermally grown pad oxide and LPCVD silicon nitride film was first formed on the wafer surface. Using DUV lithography and plasma etching, the film stack was patterned defining active areas. Exposed silicon areas were etched to form trenches with tapered side-walls. The liner oxide film was thermally grown on the trench surface and the trenches were filled by the deposition of LPCVD TEOS oxide. Some structures were annealed in dry oxygen at different conditions. This followed by CMP, the hard mask served as a stop layer for polishing. Then opened nitride patterns were removed in a hot phosphoric acid. STI processing was accomplished with the strip of the residual pad oxide from the surface of active areas using precise etching in diluted hydrofluoric acid. Devices were fabricated in active areas of STI structures using the conventional retrograde-well 0.25 μm CMOS process technology.

Crystal defects in STI structures were analyzed with an optical microscope after removing all the surface layers and defect delineation by Wright preferential etching. Transmission electron microscopy (TEM) was also applied for defect identification and the detailed study of their distributions in layout-specific device areas.

Thermomechanical properties of silicon nitride and gap-fill oxide films were determined by wafer curvature measurements at different temperatures. The laser beam stress measurement machine FSM 128 was utilized for that.

The TSUPREM-4 process simulator was used for studying the stress evolution in silicon structures. The VISCOUS simulation model was applied. It enabled stress calculations taking into account the viscous flow of materials during STI formation.

RESULTS AND DISCUSSION

Observation of dislocations

Stress-induced dislocations were consistently observed during the analysis of crystalline quality of silicon structures with STI at different stages of the device manufacturing process. The defect density was the highest in the structures inspected after source/drain formation. The first dislocations were detected at the stages of trench filling. Considering these as the processes responsible for dislocation generation onset, the major attention in this work was paid to the defect analysis during STI processing, i.e. before the formation of transistor structures.

The average density of crystal defects in random regions of STI structures was usually not high enough for defect investigation using transmission electron microscopy (TEM). Preferential etching technique revealed defects which were usually observed in an optical microscope as single etch pits similar to those shown in Fig.1 at the edges of quadrate active areas. However, in some large device elements separated by narrow trenches, considerable number of defects could be found. This case is also represented in Fig. 1. As it can be seen, these defects tended to localize at the trench corners.

Based on these observations, corner-intensive structures with a meander isolating trench having a width of 0.4 μm were studied. They seemed to be more vulnerable to defects and were regarded as an indicator of the defect generation intensity in STI processing.

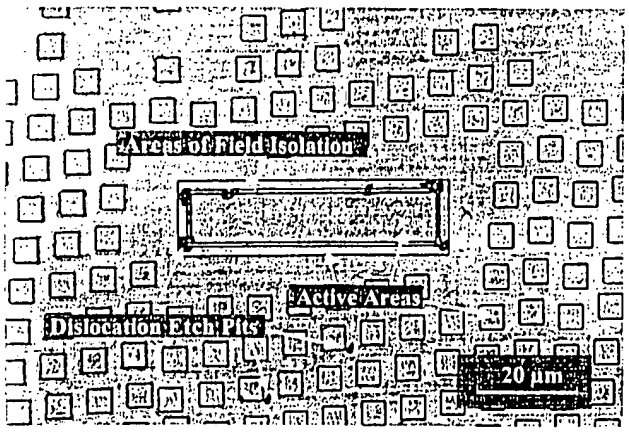

Fig.1. Optical micrograph of a randomly chosen silicon STI structure, in which dislocations were revealed using the technique of preferential etching.

Such a device with high density of defect-related etch-pits is shown in Fig.2. From the analysis under an optical microscope, it followed that the defect density at the trench corners was significantly higher.

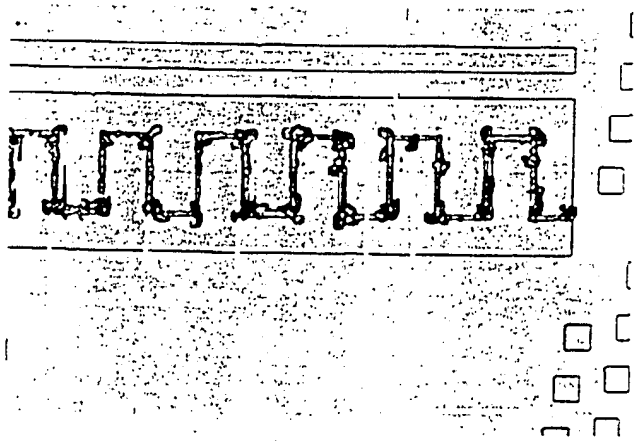

Fig.2. Optical micrograph of dislocations revealed by preferential etching in STI structures with a meander layout of isolating trench.

Using TEM, these defects were identified as dislocations. It is seen in Fig. 3 that at the strait STI segments dislocations form the kind of pile-up configurations in which they are parallel to the trench edges. Fig. 4 clearly shows that these dislocations often come out onto the upper surface of device elements when approaching the trench corners.

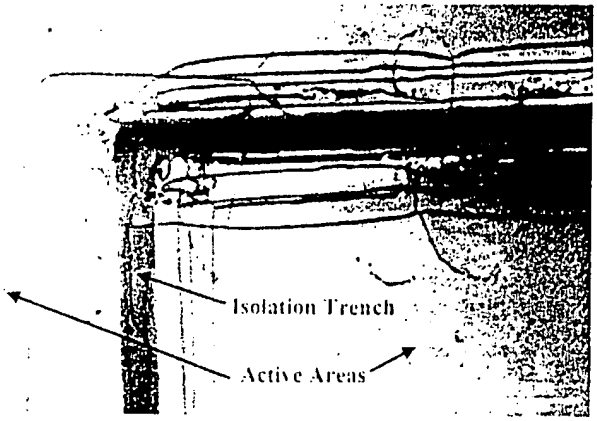

Fig.3. TEM micrograph of the STI structure with a meander isolating trench having high density of dislocations.

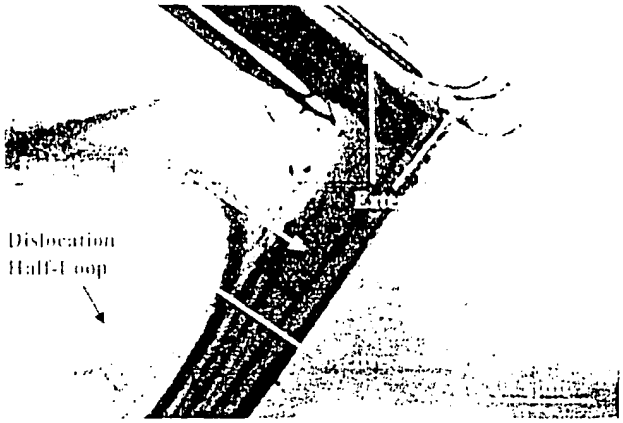

Fig.4. TEM micrograph of the STI structure with moderate density of dislocations.

Therefore, TEM observations corrected the results of optical microscopy regarding defect distributions. It showed that dislocation density is similar in all regions surrounding isolation trenches, though - due to the specific location and orientation of dislocations - preferential etching reveals them mostly at the trench corners where they come out onto the planar device surface. If dislocations come out of silicon on the sidewalls of STI trenches, one may not be able at all to detect them using the technique of preferential etching and optical microscopy. For example, single dislocation etch pits were often observed in device elements under an optical microscope, although dislocation half-loops are supposed to be revealed as pairs of etch pits.

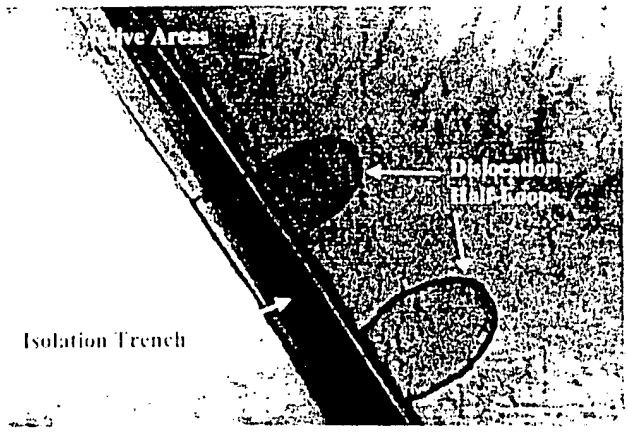

Fig.5. TEM micrograph of the STI structure with low density of dislocations.

Another important result of the TEM study relates to the features of defects when their density is low. Not strait segments but sub-micron dislocation half-loops similar to those shown in Fig. 4 and Fig. 5, were always observed in these cases. Apparently, they corresponded to the initial stages of dislocation generation. The fact that these dislocations were located at the strait elements of isolating trenches says that trench corners do not play any specific role in the dislocation nucleation. Hence, 2-dimensional stress analysis using the approximation of plane-strain is relevant for the analysis of critical stages responsible for dislocation generation during STI processing.

The "Stress Intensity" concept

The analysis of stresses in semiconductor device structures is quite a complex task. The stress fields in question are extremely non-uniform having gradients of an order of 1 GPa/μm (6). There are no experimental methods for measuring such stresses with the adequate resolution, and most research works have been relying on stress calculations. Fortunately, well-established 2-dimensional simulation tools using stress-dependent models of typical device fabrication processes are now available. They compliment the study of stress-induced defects in microscopic device structures providing realistic data on stress distributions. As soon as the stress state of a structure is determined, however, another question rises – what reasonable criteria should be used for linking the stress and device structure vulnerability to defects.

It is known that the dominating glide systems for dislocations in silicon are planes {111} with <110> directions and that silicon exhibits plastic deformation at temperatures above 600°C. However, there is much uncertainty with respect to critical resolved shear stress σ_c of dislocation formation in silicon. The lowest assessment of its value might correspond to the threshold stresses of dislocation movement. These can be as low as 0.3 MPa for the long strait dislocations in a pile-up configuration (7). To form an extended dislocation structure, some excessive stresses are needed. The upper yield stress of silicon could be considered as their estimate. Experiments on macroscopic deformation of silicon give the values of an order of 10 MPa for the conventional temperatures of device fabrication (8). Yet macroscopic plastic deformation implies the existence of multiple dislocation sources that is not the case for dislocation generation in sub-micron areas. Hence, σ_c pertinent to conditions of VLSI device processing should be higher. S. M. Hu gives for it a value of about 0.1 GPa subject to the presence of point defects, their clusters and other factors (9). The generation of point defects may enhance the formation of dislocation nuclei during local oxidation of silicon (10). Nevertheless, LOCOS structures can normally endure localized stresses of a few hundred MPa without dislocation generation (11). The correlation obtained by P. Smeys et al. on the stress level and leakage currents for the devices with LOCOS isolation, indirectly reveals the interval of 0.1 - 1.0 GPa for σ_c (12). The specific σ_c = 0.7 GPa was derived by S. Ikeda et al. from the analysis of crystalline quality and stress state modeling for the device structures produced using different LOCOS schemes (13). In the present work, two values of the critical stress level have been arbitrary chosen – 0.5 GPa and 1.0 GPa. They were treated as the lower and upper estimates of σ_c and used as the criterion for stress-induced defect formation in silicon structures with STI.

Dislocations in LOCOS structures have traditionally been interpreted as the defects formed during oxidation, that is at high temperatures. However, the evidence was recently obtained by the authors that even in LOCOS processing, the most intensive dislocation generation may occur at the time of temperature decrease when the actual

oxidation is already completed [9]. The authors believe that the chosen values of τ_{cr} do correspond to the critical stress rate of dislocation generation onset in STI structures, which, as it will be shown later, is centered within the lowest temperature interval of silicon plasticity. Therefore, independently on the processing temperature, the same τ_{cr} was considered for the identification of the critical stress rates in STI structures. Besides, the dependence of τ_{cr} on temperature may not be very strong, similar to that of the critical stress of dislocation movement in silicon [14]. Hence, the temperature dependence of τ_{cr} was assumed not to affect the conclusions of the qualitative comparative analysis performed.

Yet the relevance of σ_{cr} as a criterion for dislocation generation onset is questionable when it is used for the structures with highly non-uniform stress distributions. In their previous work, the authors analyzed σ_{cr} distributions in LOCOS structures trying to explain the cases of layout-dependent dislocation generation encountered (15). Different device elements in a silicon chip were found to be under the stress of a maximum level. In spite of this, localized dislocation assemblages were formed only in the layout-specific regions where these high stresses engaged the largest areas of silicon. Accordingly, vulnerability of STI structures to stress-induced defects has in the present work been qualitatively evaluated in terms of the area-intensive derivative of a stress field - "Stress Intensity". It was calculated as the silicon area of a 2-dimensional model STI structure where shear stresses, in at least one of the glide systems of silicon, exceeded σ_{cr}. Every stage of STI processing was simulated and stresses were examined in the temperature interval from 600°C to the highest temperature of a particular device fabrication step.

Mechanical properties of materials

Characteristics of an STI physical structure which control stresses and, therefore, stress-induced defect formation, include geometric parameters and mechanical properties of the materials integrated in STI. In this study, the major attention was paid to the thermomechanical interaction of STI structural elements, assuming that it played the dominant role in stress development and defect formation. Mechanical properties of silicon and thermally grown silicon oxide are known not to be very sensitive to methods of their fabrication. Adversely, CVD oxides demonstrate different properties and considerable changes in their density during high temperature treatments (16). Thus, mechanical characteristics of CVD oxide films used for STI trench filling had to be determined for adequate calibration of the simulation models used.

Fig. 6 represents the data on intrinsic stresses measured in TEOS CVD films. They were deposited on the blank wafers using the same conditions as those in STI processing. As-deposited films had tensile stresses of a significant level. The dependence of these stresses on the temperature of measurements showed a hysteresis, which was apparently associated with the film densification. During the temperature ramp-up, the stress decrease occurred at about 750°C manifesting the start of densification. The stresses were sensitive to the state of a wafer surface. They were slightly higher in the films deposited on the bare silicon compared with those on the wafers with previously grown 200Å thermal oxide. However, high-temperature treatments, aiming deliberate densification of the film material, brought the films up to a state at which they demonstrated similar stresses regardless deposition conditions applied. Furthermore, the stresses in annealed films became stable and almost identical independently on the annealing scheme of a reasonable choice with a temperature higher than 1000°C and process duration exceeding 15 minutes.

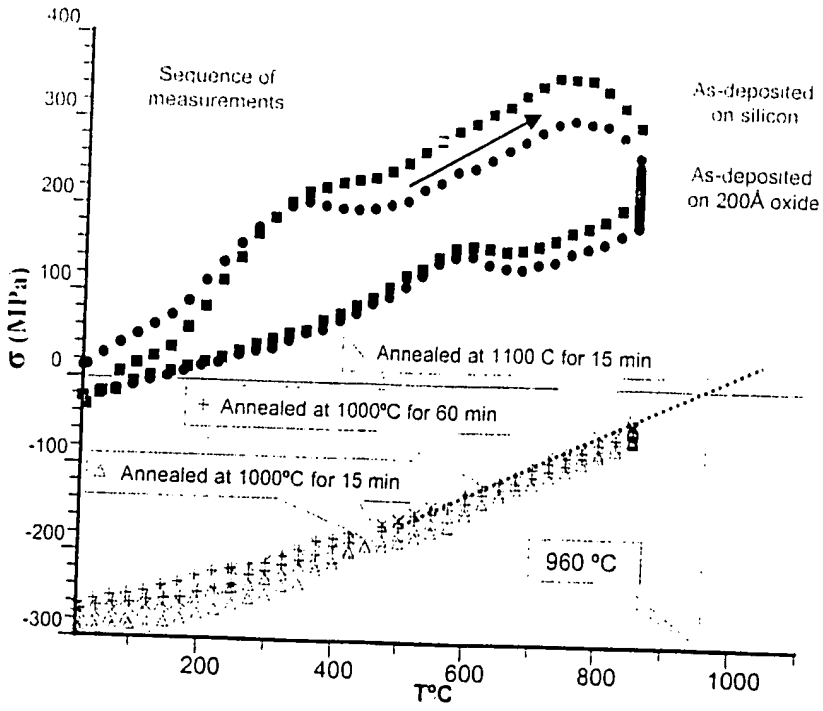

Fig.6. Intrinsic stress in LPCVD TEOS films, as-deposited and densified at different conditions, as a function of measurement temperature.

The slope of the stress-temperature curves shows the difference between the linear coefficients of thermal expansion of silicon and the film material. For the annealed films, this difference is $(0.3 - 0.39)\cdot 10^{-6}$ K^{-1} within a temperature interval of 600 - 850°C. This is close to what would be expected in the system of thermal oxide on silicon. Extrapolation of these curves to the level of zero stress gives the temperature of about 960°C that coincides with the temperature which is sometimes treated in practice as the critical point of oxide transition to viscous behavior [17]. Accordingly, stresses in STI structures were simulated assuming that post-deposition annealing causes the transformation of a gap-fill material to a state at which its mechanical properties are similar to the properties of thermally grown silicon oxide and its intrinsic stresses relax fast to a zero level at the temperatures higher than 960°C.

Based on the results of trivial measurements of stresses in silicon nitride films, silicon nitride was considered in simulations as an elastic material with the same linear coefficient of thermal expansion as that of silicon, and intrinsic tensile stress of 1.18 GPa. Other material parameters used in the computations corresponded to the default values of the simulation tool used.

Stress Evolution in STI Structures

Fig. 7 represents simulation results on "Stress Intensity" for six characteristic stages of STI processing. The silicon areas, in which resolved shear stresses, in at least one of the glide systems, exceeded 0.5 GPa, are shaded lightly. Dark shadow shows the areas with shear stresses of 1.0 GPa and above.

The first indication of high stresses in the sequence of STI processing steps was noticed at the stage of liner oxide growth (Fig 7, b). However, this process is similar to those employed in conventional LOCOS technologies and, therefore, defect generation may normally be avoided. Moreover, the stress decreases at the next step when the gap-fill oxide is deposited (Fig 7, c). The later is attributed to the tensile intrinsic stresses in the gap-fill oxide, which compensate the stress created by the growing liner oxide.

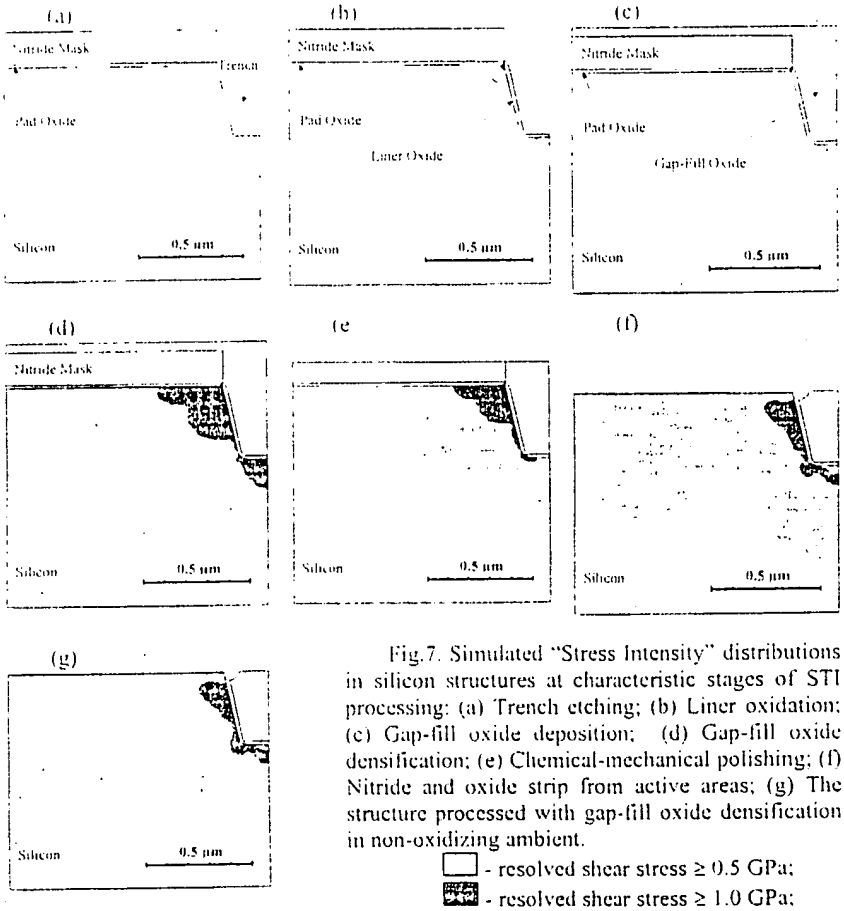

Fig.7. Simulated "Stress Intensity" distributions in silicon structures at characteristic stages of STI processing: (a) Trench etching; (b) Liner oxidation; (c) Gap-fill oxide deposition; (d) Gap-fill oxide densification; (e) Chemical-mechanical polishing; (f) Nitride and oxide strip from active areas; (g) The structure processed with gap-fill oxide densification in non-oxidizing ambient.

□ - resolved shear stress ≥ 0.5 GPa;

▨ - resolved shear stress ≥ 1.0 GPa;

Exceptionally high stress in the simulated STI structures was detected after the gap-fill oxide annealing. The annealing process itself causes gap-fill oxide densification, which is accompanied by the relaxation of intrinsic stresses. However, the mismatch of the thermal expansion coefficients of silicon and gap-fill oxide gives rise to stress development during the subsequent processes of STI formation carried out at the temperatures below 960°C. The next processing stages, CMP (Fig 7, e) and even nitride/oxide strip from the active device surface (Fig 7, f), did not change the stress notably. The correspondent "Stress Intensity", the values of which are summarized in Table I, was extremely high. It points at the process controlling the onset of critical stress states of STI structures. This is gap-fill dielectric annealing.

Table I. Simulated values of "Stress Intensity" at σ_c=0.5 GPa (I_a) and σ_c=1.0 GPa (I_b) in silicon structures at characteristic stages of STI processing.

STI Processing Stage	I_a (10^{-3}μm)	I_b (10^{-3}μm)
(a) Trench etching	22	0
(b) Liner oxidation	28	0.3
(c) Gap-fill oxide deposition	13	0
(d) Gap-fill oxide annealing	657	66
(e) Chemical-mechanical polishing	291	33
(f) Nitride and oxide removal from active areas	590	29
(g) the same as (f) but with gap-fill oxide annealed in non-oxidized ambient	594	31

Oxidation of a profiled silicon surface, which gives constrains for growing oxide expansion, is often regarded as a major contributor to stress development in the structures with trench isolation [18, 19]. In particular, the stress caused by oxidation of trench sidewalls was considered to be responsible for dislocation density increase in STI structures when oxidizing ambient was used for gap-fill oxide annealing [3]. However, the present analysis showed that there was no significant difference observed in "Stress Intensity" between the structures with simulated gap-fill dielectric densification in oxidizing and non-oxidizing atmosphere (Fig 7, g). It appears, therefore, that the contribution of the trench sidewall oxidation to stresses may not be as essential as its impact on the defect nucleation or the stress relaxation in the gap-fill oxide.

The maximum levels of "Stress Intensity" (Fig 7, d-g) in STI structures correspond to 600°C, that is the lowest temperature at which silicon exhibits plasticity through dislocation generation. The root cause of the stress rise is the mismatch of the linear coefficients of thermal expansion of silicon and gap-fill oxide. The unusual feature of the revealed stress evolution in STI structures is that the more thorough relaxation of intrinsic stress in as-deposited gap-fill oxide is achieved during its post-deposition annealing, the higher stresses are developed afterwards at lower processing temperatures. During the post-deposition annealing, the stress relaxation in gap-fill oxide occurs concurrently with its structure densification. This presents one of the challenges of STI technology optimization in terms of the trade-off between the stability of gap-filler (etch rate, volume shrinkage and so on) and silicon structure immunity to stress-induced defects.

SUMMARY

Crystalline quality of silicon structures with shallow trench isolation (STI) has been studied. Dislocation etch pits were observed on the surface of the structures in an optical microscope after preferential etching. They tended to localize at isolation trench corners. Transmission electron microscopy proved that the etch pits corresponded to dislocations. At the same time, indications were found that dislocations nucleate at the sidewalls of strait STI segments, not at the corners. This justified using 2-dimensional stress simulations in the search for the processes responsible for the development of the critical stress states of a dislocation generation onset in STI structures.

Mechanical properties of LPCVD TEOS oxide, which was used as gap-fill dielectric in STI processing, were determined experimentally. It was found that as-deposited oxide films had high tensile stress. It relaxed during the high temperature annealing followed the gap-fill oxide deposition. The applied simulation models were calibrated accordingly.

From the previously reported data on the conditions of dislocation generation onset in the micro-volumes of silicon devices, the criterion was derived for the assessment of STI structure vulnerability to stress-induced defects. It was described in terms of "Stress Intensity" as the area of a device structure where shear stresses, in at least one of the glide systems of silicon, exceed 0.5 - 1.0 GPa at temperatures higher then 600°C.

The simulation results show that the stress development is mainly controlled by the gap-fill oxide annealing. The "Stress Intensity" risen at this stage is the highest and does not change significantly during the subsequent processes. The related stress state of STI structures is realized within the temperature interval of 600 - 900°C, which is unavoidable in device fabrication. The better densification of gap-fill oxide is achieved, the more vulnerable STI structures become to dislocation generation. On the other hand, gap-fill oxide densification improves surface morphology of device structures as it prevents the revealing of seams in gap-fill oxide and the recess of STI regions. This presents the complicated trade-off between the crystalline quality and surface planarity of STI structures. The best solution for stress-related problems of STI may be found in the search for the gap-fill materials with controllable level of residual tensile stress, which would be stable during high temperature treatments.

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COP Induced Isolation Failure in CZ Si Wafers

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The presence of COPs on the 64MRAM device isolation region causes the current path between neighbor transistors, which called the COP induced isolation failure. The probability of the COP induced isolation failure depends on the COP size; i.e., larger COP size leads to higher probability. In addition, it strongly depends on the process condition of the isolation structure such as the nitride film thickness; i.e., thicker nitride film leads to less probability. Furthermore, it depends on isolation structure; i.e., higher probability of the COP induced isolation failure follows LOCOS > PSL > SEPOX

INTRODUCTION

In sub-micron DRAM devices, the design of material properties fitting the device design rule is likely a key engineering activity to achieve a high device yield and reliability. A major material property affecting device characteristics is surface crystal defects such as COPs, large dislocation, and Oxidation Induced Stacking Fault Ring(O.I.S.F.-ring). Particularly, a main surface defect on Czochralski silicon wafers is Crystal Originated Particles (COPs). COPs are the square-shape surface pits with {111}, originated from D-defects, truncated octahedral void, formed during Czochralski silicon single crystal growth [1-18]. It has been known that COPs degrade the gate oxide integrity [19-29] and produce the device isolation failures [30]. In this study, the mechanism by which COPs cause the device isolation failure is discussed. In addition, the dependency of the isolation structure on the device isolation failures is investigated.

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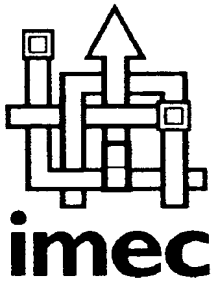

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Investigation of Stress in STI using UV-Raman Spectroscopy

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Abstract

We present an investigation of local mechanical stress in shallow trench isolation (STI) by UV-Raman spectroscopy. UV light penetrates only 15 nm into silicon and allows to monitor the stress very close to the surface. In this way, local areas of high stress, averaged away by longer wavelength light used in conventional Raman spectroscopy, can be detected. Using this UV-method, we show that wet densification introduces large compressive stress in the trench corners and may lead to defect 'creation, especially in small trenches.

1. Introduction

Raman spectroscopy has proven to be a valuable tool to investigate mechanical stress in silicon microelectronic device structures [1]. It is possible to measure stress after subsequent process steps and thus follow its evolution. The conventional way up to now has been to use the 458 nm line of an Ar^+-ion laser for excitation of the Raman signal. The light penetrates up to 300 nm deep into the silicon, and the stress measured is therefore a weighted average over this depth. We recently managed to perform Raman measurements with UV (364 nm) excitation [2]. The major improvement is the greatly reduced penetration depth, which is with UV only ~15 nm, so the stress measured is the true stress at the silicon surface. We applied this improved method to study the mechanical stress introduced into the silicon by a shallow trench isolation (STI) process. First, we will give a short review on stress measurements with UV-Raman spectroscopy and demonstrate the improvement of UV over visible light excitation. Then we follow the evolution of stress through the first few steps of our STI process up to the filling of the trenches by TEOS deposition. Different TEOS parameters and their influence on the stress will be discussed.

2. Experimental

2.1. UV-Raman spectroscopy

Figure 1 shows a typical Raman spectrum of the Silicon phonon at 521 cm^{-1}. The spectral frequency (Raman shift) of this phonon is influenced by mechanical stress and shifts according to the sign and magnitude of stress. A negative shift indicates tensile stress and a positive shift compressive stress. Placing the sample

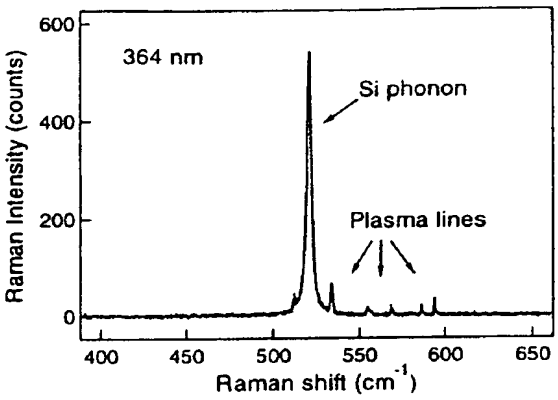

Figure 1. Raman spectrum of unstrained Si with the Si phonon at 521 cm^{-1}. The small lines are plasma lines from the Ar^+-ion laser.

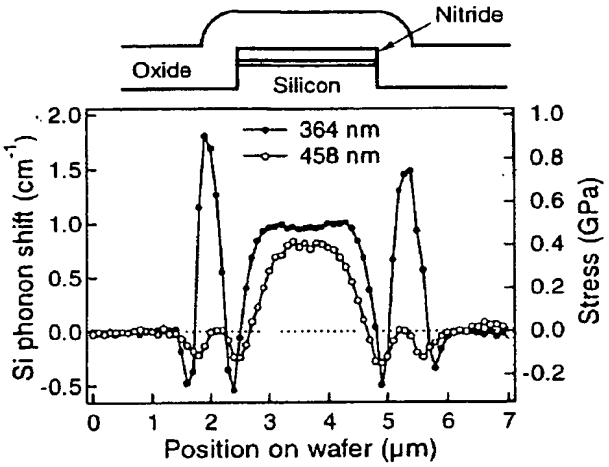

Figure 2. Comparison of stress patterns obtained with blue (458 nm) and UV (364 nm) light. The sample structure is shown schematically at the top. The stress values labelling the right axis were calculated assuming uniaxial stress.

under a microscope allows to measure the stress locally resolved with almost diffraction limited resolution. For 458 nm excitation the laser spot on the sample is about 0.9 µm and for 364 nm light 0.7 µm. The penetration depth of the light into the sample depends on the absorption strength for the given wavelength of light. For UV light the energy coincides with the direct transition in silicon at the Γ-point. Therefore, absorption is very high and the penetration depth is reduced to ~15 nm as compared to ~300 nm for blue excitation. The stress measured at a certain position on the wafer is averaged over the finite laser spot size and over the penetration depth. Reducing the penetration depth to a minimum allows to measure stress very close to the surface. Thus, we are able to pinpoint local areas of stress, which are not detected by longer wavelength light, because they are averaged away in the latter. A demonstration of this is given in Figure 2. The traces in the figure were obtained by moving the sample under the microscope in steps of 0.1 µm and recording a Raman spectrum as in Fig. 1 for every position. Plotting the shift of the Si phonon over the position on the wafer leads to the graph shown in Fig. 2. The sample structure investigated is shown schematically on top of the figure. The stress values given on the right axis are calculated assuming uniaxial stress [1]. The details of the stress patterns will be discussed in the later sections.

2.2. Sample preparation

The isolation mask is prepared by depositing a 200 nm LPCVD nitride film on a 20 nm-thick pad oxide. After photolithographic definition of the active area, the nitride /oxide stack is etched and 380nm deep trenches are subsequently etched into the silicon substrate. After cleaning, a 20 nm thick sidewall oxidation is performed at 1050°C. Next, a flowable oxide (a hydrogen silsesquioxane spin on dielectric, HSQ) is deposited by spin coating and is cured at 850°C in oxygen.

This provides enough sloping of the trench profiles to allow a void-free bulk fill with LPCVD TEOS. Finally, a 550 nm thick LPCVD TEOS capping is deposited and densified at 850°C in steam ambient or at 1050°C in dry oxygen.

3. Stress in STI

STI is the key isolation technology for sub-micron CMOS devices. As device dimensions keep decreasing, the gap-fill process and the thermal cycles become more critical. The main concern of as-deposited gap-fill materials, is their high etch rate in HF solutions as compared to thermal oxide. Densification, especially when using steam ambient, improves the etch rates. Stress on the underlying silicon, coming from the gap-fill material as deposited or appearing as a result of its densification, may lead to defect creation.

In this section we will show the evolution of mechanical stress in arrays of trenches with different width and spacing. Figure 3 shows the stress measured after re-oxidation of the trench walls. The line array consists of groups of 10 lines each with variable width and spacing. The rightmost group has a width and spacing of 3.0 µm. Going to the left, the dimensions are 2.0, 1.0, 0.9, 0.8, 0.7, 0.6, 0.5, 0.45, 0.4 and 0.35 µm. The groups are separated by 5 µm wide trenches. These dimensions also apply to Figures 4 and 5.

It is obvious that the trench dimension has a large impact on the stress levels. Within the 3.0 µm line group, the maximum compressive stress is in the line under the nitride. This behaviour has been investigated in detail in previous publications [3]. As the lines become narrower, the stress under the nitride increases up to the 1.0 µm group. From then on the stress decreases again, until it even becomes negative (tensile) below 0.5 µm. The increase and decrease of stress can be understood by mechanical considerations in combination with the averaging due to the finite laser spot [4]. The influence of different densification parameters can be seen in Figures 4 and 5. Comparing e.g. the 3.0 µm line group in Figs. 3 and 4, a new area of high compressive stress can be seen besides each line in Fig. 4. One of those 3 µm wide lines of Fig. 4 is shown in more detail in Fig. 2.

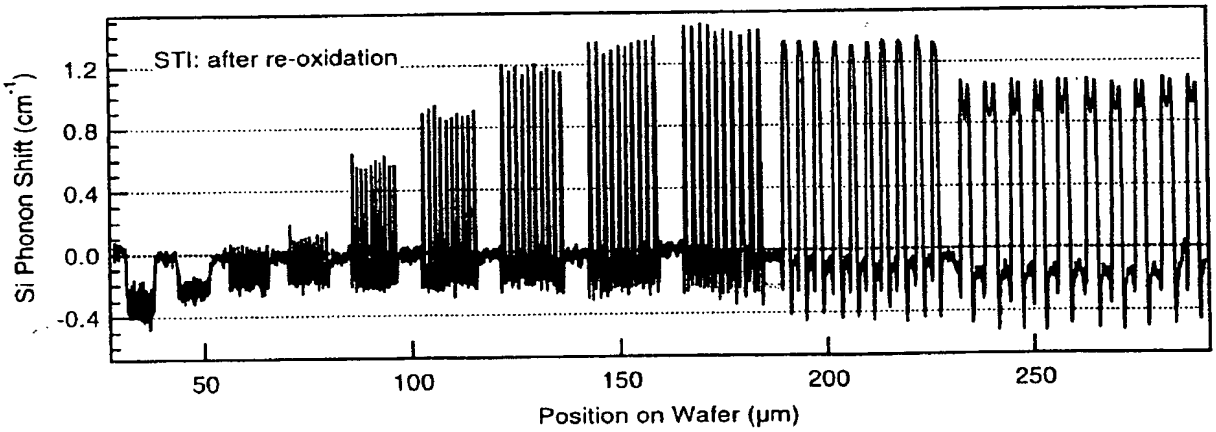

Figure 3. Mechanical stress in line arrays after trench etch and re-oxidation of the sidewalls.

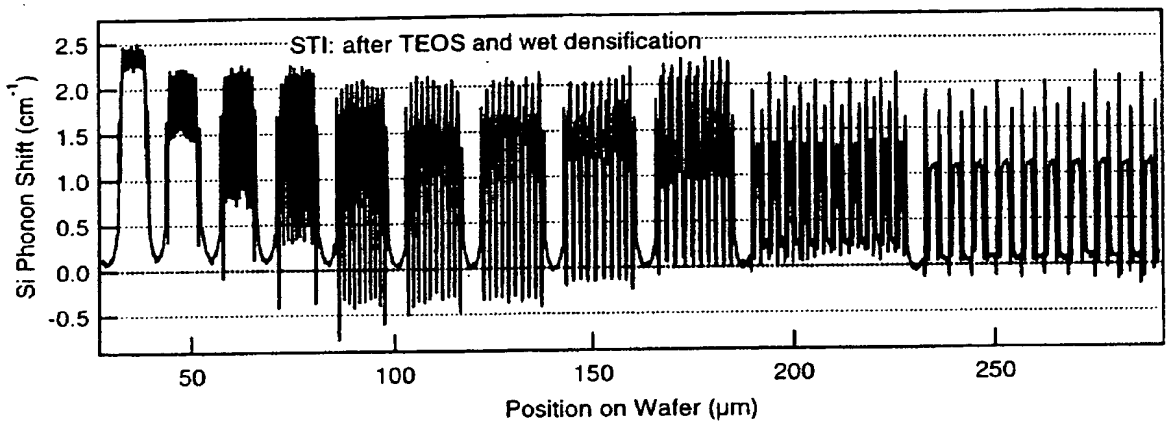

Figure 4. Mechanical stress in line arrays after TEOS and wet densification.

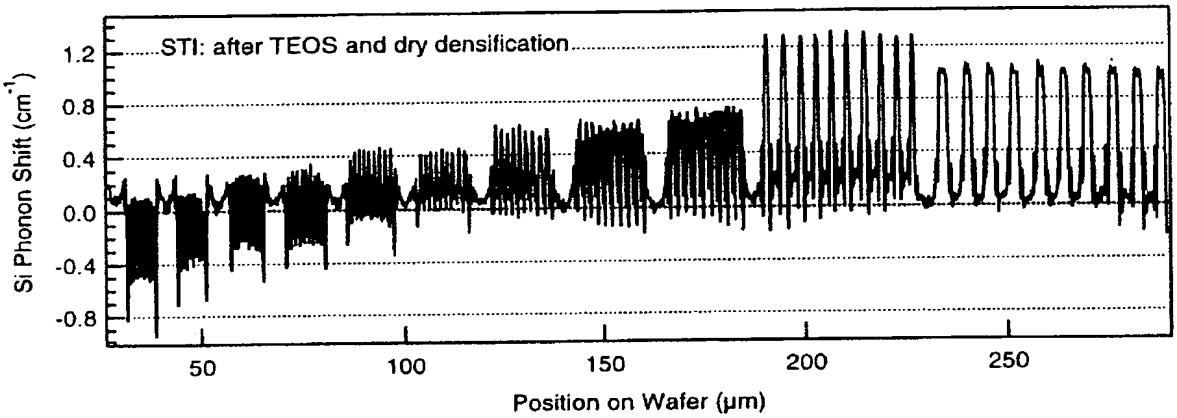

Figure 5. Mechanical stress in line arrays after TEOS and dry densification.

This additional stress component is not present when using dry densification, as can be seen in Fig. 5. Whereas in Fig. 5 the stress under the nitride decreases from the 1.0 µm line on, in Fig. 4 the stress is mostly determined by the additional compressive stress from the wet densification. We thus proved experimentally that wet densification results in a severe stress increase which may lead to defect formation in the trench corners, especially in small trenches.

4. Conclusion

We have shown that mechanical stress in STI depends strongly on the densification mechanism. UV-Raman is a powerful tool to follow the evolution of stress after different processing steps. The usage of UV light for excitation reduces the penetration depth in silicon to 15 nm. Therefore, only the true surface stress is measured. We believe that this method will play an increasing role in the determination of suitable process parameters to minimise mechanical stress and the potential for defect formation.

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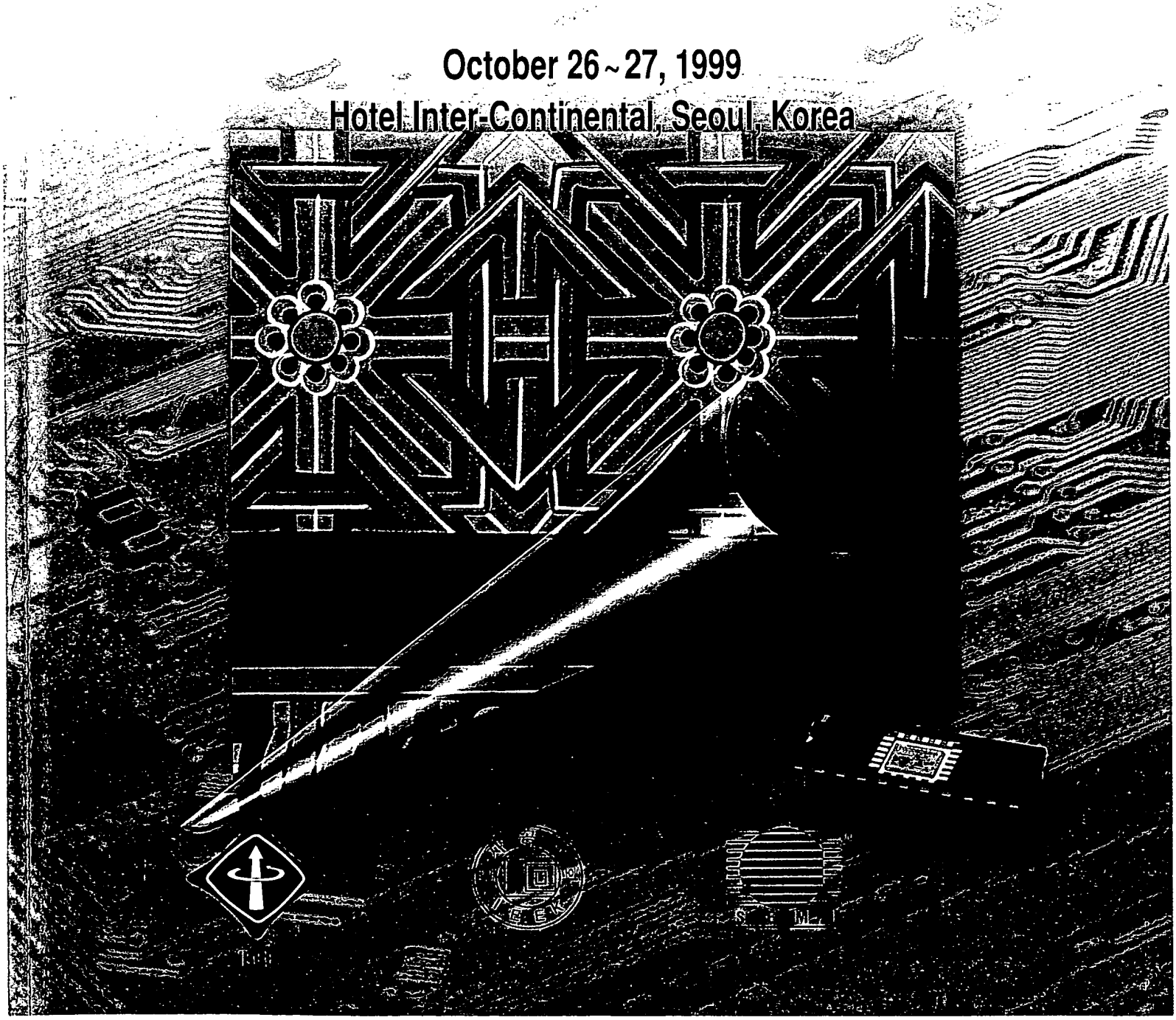

HIGH DENSITY LOW POWER FULL CMOS SRAM CELL TECHNOLOGY WITH STI AND CVD Ti/TiN BARRIER METAL

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ABSTRACT

A novel Full CMOS SRAM cell had been developed for low power applications. The cell size is 5.038μ $m^2$with 0.2μ m design rule. Extremely low standby current was achieved by adopting the continuous active patterns in the cell layout to reduce STI induced leakage current by minimizing the STI induced stress compared to conventional isolated active cell. Also, the feasibility of CVD Ti/TiN barrier metal for filling the deep small contacts had been proven for the first time. 8M bits low power slow SRAM was developed sucessfully using this technology.

INTRODUCTION

According to rapid development of hand held machines, the demands of super low standby current and higher packing density are simultaneously growing. In order to satisfy increasing packing density the minimum feature size of isolation is greatly reduced by adopting a STI (Shallow Trench Isolation) Technology. However , the STI is known to generate higher mechanical stress, which causes defects, such as dislocation[1~3]. These defects become major sources of leakage current. Therefore, minimizing trench-induced stress is a key challenge to achieve a super low standby current SRAM. The magnitude of the stress depends on not only IC processes but also active pattern shapes. Therefore, in this study, SRAM cells with two different active layouts were compared to investigate the relationship between the leakage current and the active pattern of the cell. In addition to the STI, a barrier metal filling technology of small contact holes, which are less than 0.2μ m, is another critical issue to solve the requirements of low contact resistance and low contacted junction leakage current in low power SRAM products. CVD Ti/TiN barrier metals was implemented

PROCESS INTEGRATION

The layouts of the CA(Continuous Active) SRAM cell and conventional IA(Isolated Active) cell are shown in Fig.1 Also, the top view SEM photographs of both cell types are shown in Fig.2. The CA cell size is 5.038μ m^2(1.88μ m X 2.68μ m), when 0.2μ m design rule is used.The conventional IA cell has almost the same size, 5.09 μ m^2 (2.14μ m X 2.38μ m). Exactly same process technology was used for both cells. Fig 3 shows the cross-sectional SEM picture of the CA cell. 8M bits slow SRAM was fabricated. 0.35μ m depth shallow trench isolation and retrograde twin well were used for 0.32μ m space N+/N+ and P+/P+ , 0.48μ m space N+/P+ isolations. The trench was filled with O3-TEOS and then was planarized with CMP. 5nm nitrided oxide was grown as gate oxide. WSix/poly-Si polycide were used as gate materials. The minimum size of the gate length was 0.22μ m. In order to connect the cell transistors to each other in a cross coupled way , to bit lines and to power lines, the contact hole, whose bottom size was 0.2μ m, was formed after the ILD layer was deposited and planarized. Its aspect ratio was about 4. This very small and high aspect ratio contact hole was filled with Ti/TiN barrier metal using CVD method. W damascene process was used to form the local interconnections,Vss and Vcc in the cell. Al metal layer was used for bit lines

STI INDUCED LEAKAGE CURRENT

The key feature of the CA cell layout is perfectly lined and connected N+ active regions compared to the IA cell. Therefore, the major difference between the both cells is the connectivity of N+ active regions. In the IA cell the N+ active region is closed by itself in every cell. This makes an isolated big field area inside of the closed N+ active. The trench induced stress is sensitive to geometry because the thermal expansion differences, which is generated during high temperature annealing, will be accommodated differently according to the geometric shape of the trenches and Si active. The close looped active might receive stress from all directions . The big inside field may give more stress to the closed active. The higher stress will induce more junction diode leakage current in the IA cell. The junction diode leakage current was measured from both cell types and shown in Fig.4. As expected, the CA cell has less leakage current These results were confirmed again from the measured standby currents per cell from the test vehicle devices , which are shown in Fig.5.

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CVD Ti/TiN BARRIER METAL

As the size of contact hole on non-salicide Si active decreases below 0.2μ m, it becomes difficult to deposit the barrier metal into the high aspect ratio contact holes using the conventional PVD method. Therefore, here, the CVD method was tried and successfully implemented. The contact resistance was compared with that of the PVD Ti/TiN in Fig.6. The resistance of CVD is much lower and uniform. Also, the typical characteristics of the contacted junction diode leakage current is shown in Fig.7. The leakage current of CVD Ti/TiN is comparable with that of PVD Ti/TiN. The standby current portion between both methods in 8M bits slow SRAM was compared in Fig.8.

ELECTRICAL CHARACTERISTICS

The Typical transistor Vg-Id characteristic curve is shown in Fig.9 and DC measurement results are summarized in Table 1. The cell was operated stably down to 0.5V as shown in Fig.10. The standby current of 8M slow SRAM was measured less than 0.4μ A at Vcc=2.0V.

CONCLUSION AND SUMMARY

The CA(Continuous Active) Full CMOS SRAM cell had showed that leakage current can be reduced dramatically by minimizing the STI induced stress with perfectly lined and connected active pattern. Also, the feasibility of CVD Ti/TiN barrier metal for future devices with deep small contacts had been proven for the first time 8M bits low power slow SRAM was developed sucessfully using this technology.

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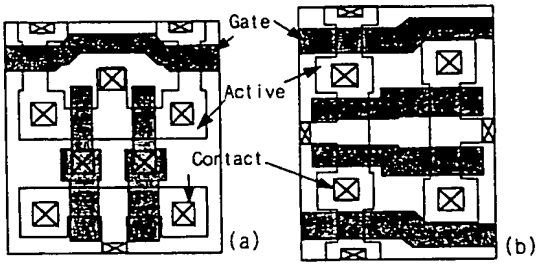

Fig.1 SRAM Cell layouts (a) IA cell, (b) CA cell

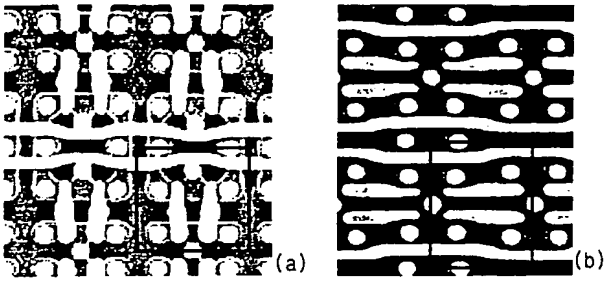

Fig.2 Top view SEM photographs after gate poly patterning (a) IA cell, (b) CA cell

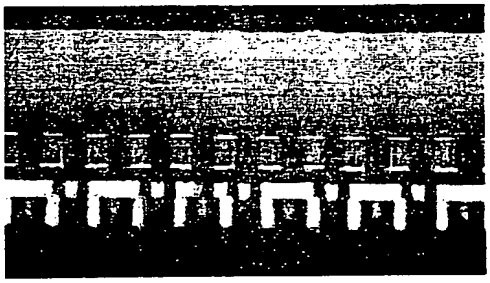

Fig.3 Cross-sectional SEM photograph of the CA cell

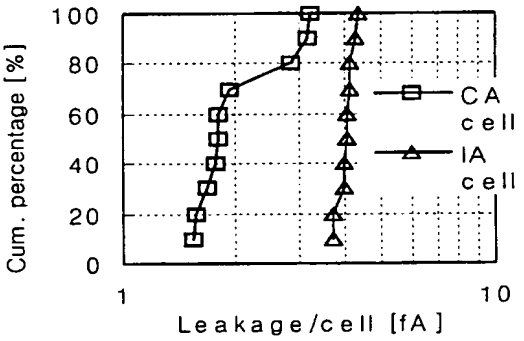

Fig.4 Junction diode leakage current (Vdd=2V) of N+ active test patterns

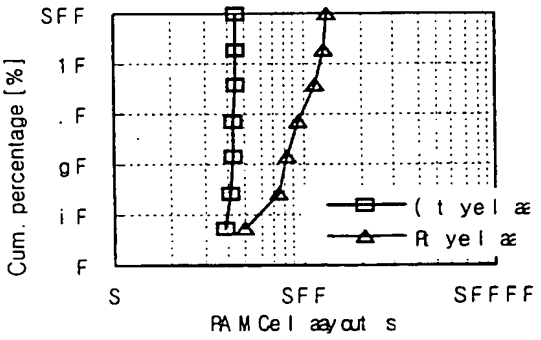

Fig.5 Standby current measured at Vdd=2V from 8M bits SRAM

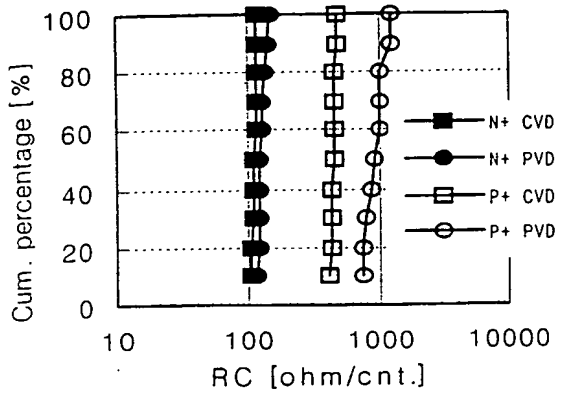

Fig.6 Contact resistance comparison between CVD Ti/TiN and PVD Ti/TiN

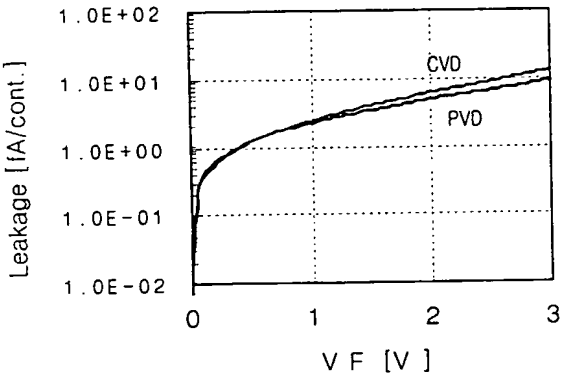

Fig.7 diode leakage current of contacted N+ active junction @2V

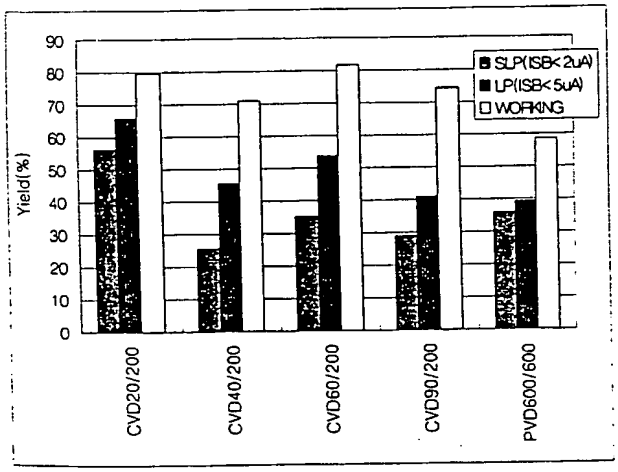

Fig.8 Standby current portion comparison between CVD Ti/TiN and PVD Ti/TiN in 8M bits Slow SRAM

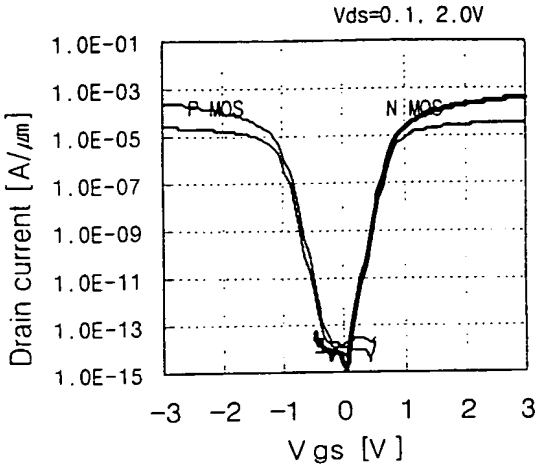

Fig.9 Vg-Id characteristics ofN,P MOS @Vds=0.1,2.0V

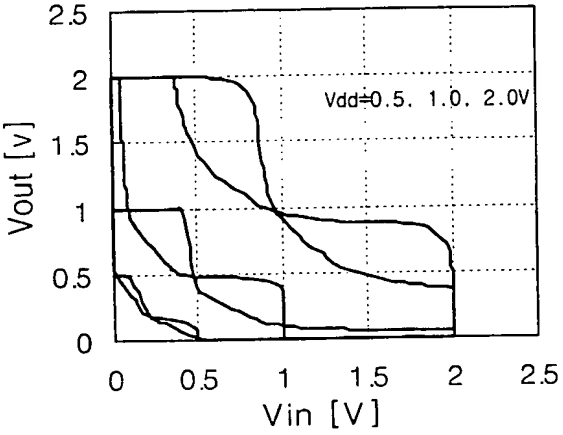

Fig.10 DC characteristics of SRAM cell @ Vdd=0.5, 1.0, 2.0V

Table.1 Device Parameter Summary

Device Parameters	NMOS	PMOS
Tox (nm)	5	5
Leff (μm)	0.12	0.20
Vth (V)	0.75	-0.75
Idsat (μA/μm) @Vds=Vgs=2V	200	-140
Idoff (Aμm) @Vds=2V	≤ 10 fA	≤ 10 fA
S (mV/decade)	85	80
BV (V) @Ileakage=1μA	≥ 8	≥ 8

[23]

Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices

Daewon Ha, Changhyun Cho, Dongwon Shin, Gwan-Hyeob Koh, Tae-Young Chung, and Kinam Kim

Abstract—**As the density of dynamic random access memory (DRAM) increases up to giga-bit regime, one of the important problems is the control of the process-induced defects and damage. Although the shallow trench isolation (STI) is widely used for deep submicron devices, it has a great possibility of generating STI dislocations due to its inherently large mechanical stress and damage. When STI dislocations are located within the depletion region of pn junction, anomalous junction leakage current could flow. This junction leakage current degrades the memory cell data retention time and the standby current of DRAM. We resolved the problems from STI dislocations as follows; the crystal defects and the mechanical stress were reduced by optimizing the implantation condition and the densification temperature of trench filled high-density plasma (HDP) oxide, respectively. In addition, the residual mechanical stress before source/drain implantation was relieved through rapid thermal nitridation (RTN). By using these methods, STI dislocations were successfully clamped outside the depletion region of pn junction.**

Index Terms—**Data retention time, dislocations, dynamic random access memory (DRAM), junction leakage current, shallow trench isolation (STI).**

I. Introduction

DYNAMIC random access memory (DRAM) devices have been developed in pursuit of the high-memory density capability and the reliable performance with the continuous shrinkage of the minimum feature size. As the memory density increases up to giga-bit regime, several challenges should be encountered and controlled very carefully: the increase of standby current due to a large chip size and the decrease of memory cell data retention time due to a small memory cell capacitor area [1]. In subquarter micron technology, shallow trench isolation (STI) has been the most predominant isolation method for many reasons that the abrupt transition of active/field region, the good planar surface, the reduced junction capacitance and the improved data sensing margin [3], [4]. Inherently large mechanical stress and damage in STI, nevertheless, combined with the subsequent process-induced stress and defects, would generate STI dislocations. In recent studies, abnormally large leakage current through junction and/or transistor was attributed to the presence of STI dislocations within the junction depletion region. Ikeda *et al.* [6] showed that the mechanical stress from device structure and source/drain annealing could generate dislocations even though LOCOS isolation method was adopted. They proposed the two step annealing for both the activation of source/drain dopant and the minimization of the mechanical stress. Ishimaru *et al.* [7] and Park *et al.* [8] proposed the technology of diminishing the residual stress in STI through the high-temperature densification and the optimized combination of trench filling TEOS-O_3 oxide, respectively. Damiano *et al.* [9] showed that the crystal defects from source/drain implantation would generate STI dislocations during the following high-temperature thermal annealing and the reduced mechanical stress alone could not thoroughly eliminate the STI dislocations. By applying an additional oxidation process after source/drain implantation, they could obtain the dislocations-free STI. In our experiment, however, the short-channel effect of PMOS transistor was significantly aggravated due to the oxidation enhanced boron diffusion.

In this paper, the behavior of STI dislocations and the effect on the pn junction characteristics during the fabrication of an experimental 16-Mb DRAM with the minimum feature size of 0.15 μm will be described in Section II. In Section III, the memory cell data retention time imposed by the anomalous junction leakage current and the technology of clamping STI dislocations outside the depletion region of pn junction without the degradation of device performance through the rapid thermal nitridation (RTN) instead of the gate reoxidation and the careful control of mechanical stress in STI and process-induced defects are discussed. Finally, conclusions are followed in Section IV.

II. Behavior of STI Dislocations

There are several factors to generate STI dislocations; crystal defects, mechanical stress and thermal annealing. During the fabrication of DRAM devices, they are reacted with other in a complex manner. Therefore, it is very helpful to investigate each factor and its role of generating STI dislocations. Crystal defects are primarily resulted from ion implantation. Although ion implantation has been indispensable by virtue of the precise control of doping concentration and profile, it induces crystal defects and needs thermal annealing for dopant activation. Several ion implantation steps are essentially adopted for fabricating DRAM devices; well, punchthrough stop, threshold voltage adjust, source/drain, and contact hole formation. Among these steps, source/drain and contact hole implantation mainly provide the seeds of STI

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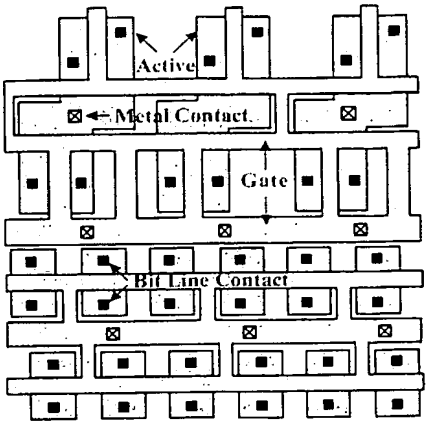
dislocations because low dose ($\leq 1 \times 10^{14}$ cm^{-2}) implantation induces a little crystal defects regardless of the dopant species [10]. In DRAM fabrication, a few thermal annealing (or oxidation) steps are necessitated for the interlayer dielectric densification and the capacitor formation. During the thermal annealing, crystal defects from ion implantation generate STI dislocation, which moves along the mechanical stress in STI and interacts with others to evolve a larger dislocation [11].

An experimental 16-Mb DRAM with the capacitor-over-bit line (COB) structure was manufactured using 0.15-μm technology node and the fabrication sequence was reported in our previous study [2]. Fig. 1 shows (a) the layout of a sense amplifier (S/A) region and the plan-view SEM images of a S/A region after strip off and wright etching (b) before and (c) after capacitor formation, respectively. Because most of the thermal annealing after source/drain implantation is accomplished during the capacitor formation, STI dislocations were investigated before and after capacitor formation. In order to observe the STI dislocations, the samples were etched using diluted HF solution and immersed in wright solution. Most of STI dislocations, confined inside the contact hole before the capacitor formation [Fig. 1(b)], have moved toward the STI corner and the STI boundary beneath the gate after heat treatment of Ta_2O_5 capacitor dielectric materials [Fig. 1(c)]. The driving force and direction of STI dislocations were generated by the thermal energy during capacitor formation and the mechanical stress in STI, respectively. Fig. 2 shows the stress simulation result of STI using TSUPREM. The maximum stress exists at the trench corner, which is coincident with previous studies [15], [16].

Fig. 3(a) shows the cross-sectional TEM image of STI dislocations. As long as STI dislocations are located outside the depletion region of junction, they could not have any detrimental effect on the pn junction characteristics. When STI dislocations penetrated the depletion region, however, they acts as the recombination/generation center between the band gap and the abnormally large leakage current of reverse-biased junction could flows through them [12]. Fig. 3(b) shows the reverse-biased leakage current of p^+n junction in an actual sense amplifier (S/A) before (filled triangle) and after (filled circle) capacitor formation. Even though a small reverse bias (<3.0 V) is applied, anomalously large junction leakage current flows especially for the case of after the capacitor formation. This result implies that the thermal annealing for capacitor formation collects the crystal defects and makes them grow vertically enough to penetrate the depletion region.



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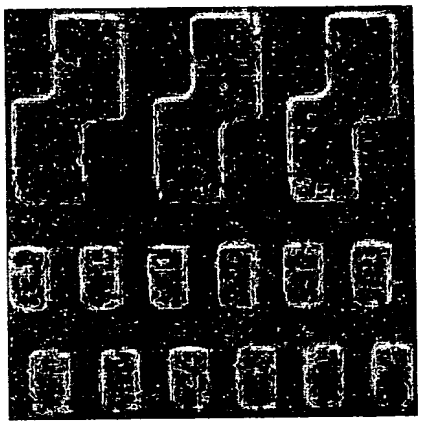

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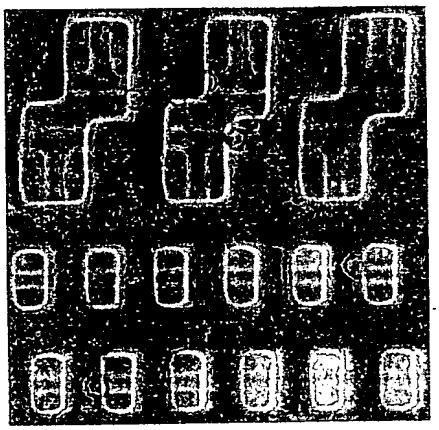


(c)

Fig. 1. (a) Layout of a sense amplifer (S/A) region and the plan-view SEM images of a S/A region after strip off and wright etching (b) before and (c) after capacitor formation, respectively.

III. Impact of STI Dislocations on DRAM Performance

The memory cell data retention time can be decreased by the large leakage current through cell transistor and storage node junction. In order to suppress the sub-threshold leakage current of cell transistor, the threshold voltage is usually adjusted around 1.0 V regardless of the DRAM density. Therefore, the substrate doping concentration should be increased with the shrinkage of the minimum feature size. Because of the increased substrate doping concentration, junction leakage current should be carefully controlled especially for the high-density DRAM [1]. The effect of junction leakage current on the memory cell data retention time can be evaluated as below.

When the cell storage capacitor has a high data (V_{CC}) and the bit lines are precharged with 0.5 V_{CC}, the total charge ($Q_{T,I}$) becomes

$$Q_{T,I} = C_S \times (V_{CC} - \Delta V_L) + C_{BL} \times \tfrac{1}{2} V_{CC} \qquad (1)$$

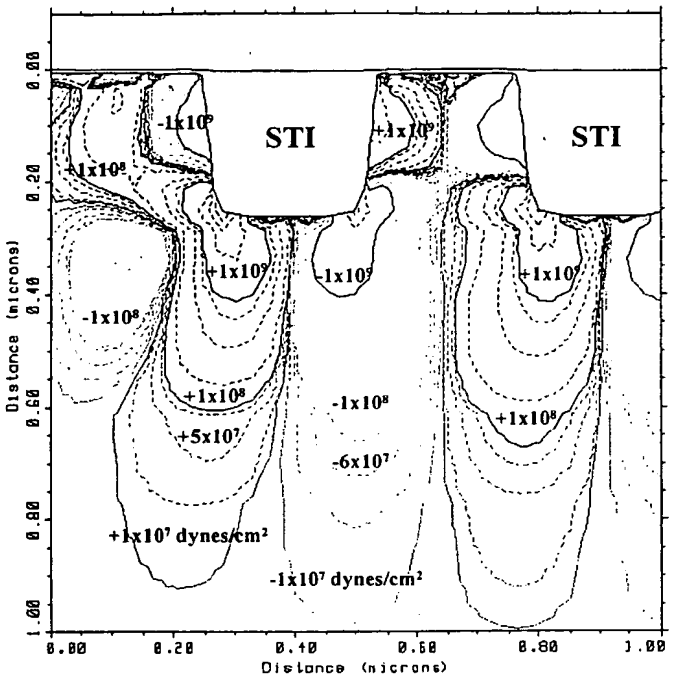


Fig. 2. Stress simulation result of STI using TSUPREM. The maximum stress exists at the trench corner.

where C_S and C_{BL} are the cell storage capacitance and the parasitic bit-line capacitance, respectively. V_{CC} is the operation voltage and ΔV_L is the data loss at the storage node due to the leakage current through junction, transistor, and capacitor.

When the memory cell is selected, the data stored in the cell storage capacitor is transferred to bit-line and the total charge ($Q_{T,F}$) becomes

$$Q_{T,F} = (C_S + C_{BL}) \times V_{BL}. \quad (2)$$

According to the charge conservation law, the total charge before charge transfer ($Q_{T,I}$) should be equal to that after charge transfer ($Q_{T,F}$). Therefore, we can obtain the bit line voltage (V_{BL}) as follows:

$$V_{BL} = \frac{C_S}{C_S + C_{BL}} \times (V_{CC} - \Delta V_L) + \frac{C_{BL}}{C_S + C_{BL}} \times \tfrac{1}{2} V_{CC}. \quad (3)$$

Since the complementary bit line is precharged with 0.5 V_{CC}, the differential voltage between two bit line (ΔV_{BL}) becomes

$$\Delta V_{BL} = V_{BL} - V_{\overline{BL}} = \frac{C_S}{C_S + C_{BL}} \times \left(\tfrac{1}{2} V_{CC} - \Delta V_L\right). \quad (4)$$

The data loss at storage node can be defined as

$$\frac{C_S \times \Delta V_L}{T_{RET}} = I_{LEAK} \quad (5)$$

where T_{RET} is the memory cell data retention time and I_{LEAK} is the total leakage current at the storage node. Using (4) and (5), the relationship of the memory cell data retention time and the leakage current at storage node can be obtained as follows:

$$T_{RET} = \frac{C_S \times \frac{1}{2} V_{CC} - \Delta V_{BL} \times (C_S + C_{BL})}{I_{LEAK}}. \quad (6)$$

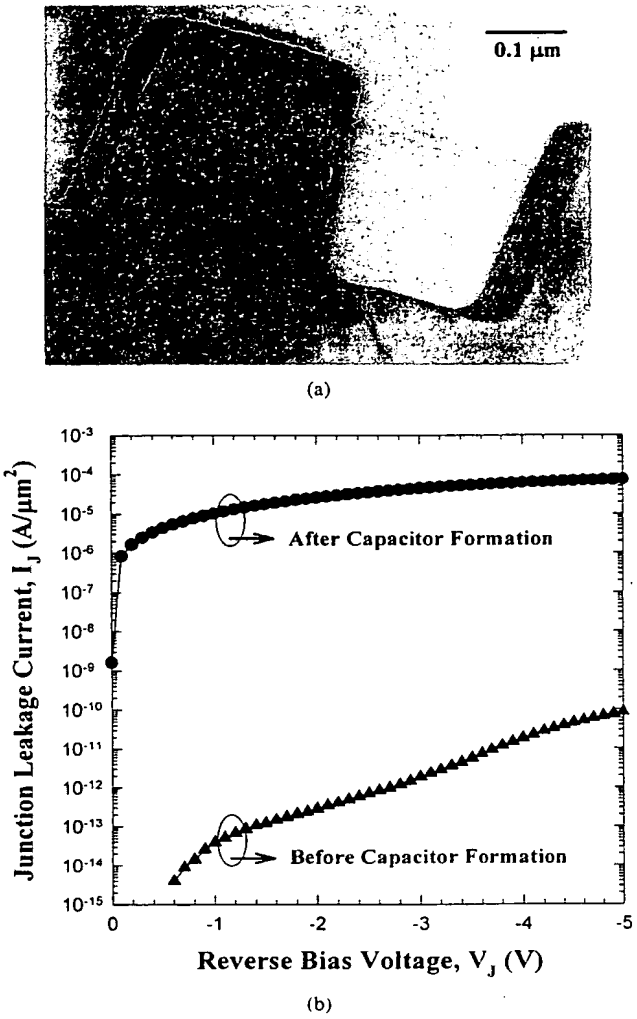


Fig. 3. (a) Cross-sectional TEM image of STI dislocations and (b) the reverse-biased leakage current before (filled triangle) and after (filled circle) capacitor formation measuring p^+n junction in an actual sense amplifier (S/A).

Fig. 4 shows the memory cell data retention time versus the leakage current at storage node with the operation voltage as a parameter. The cell storage capacitance (C_S), the parasitic bit line capacitance (C_{BL}), and the bit line sensing voltage (ΔV_{BL}) are assumed to be 25 fF, 130 fF, and 80 mV, respectively. When the leakage current at storage node is higher than 5×10^{-13} A/cell, the memory cell data retention time is considerably decreased for low voltage operation. Because the data retention time of DRAM devices is determined by weak memory cells, the refresh characteristics could be significantly aggravated by memory cells which suffer from the anomalously large junction leakage current induced by STI dislocations.

In order to eliminate STI dislocations, many efforts were concentrated on minimizing the mechanical stress in STI and the crystal defects from ion implantation. According to Ishimaru *et al.* [7], the densification of TEOS-O_3 oxide at high temperature (1200 °C) minimizes the oxide etch-rate in HF solution and the residual stress in STI at the same time, but this may induce other problems such as wafer

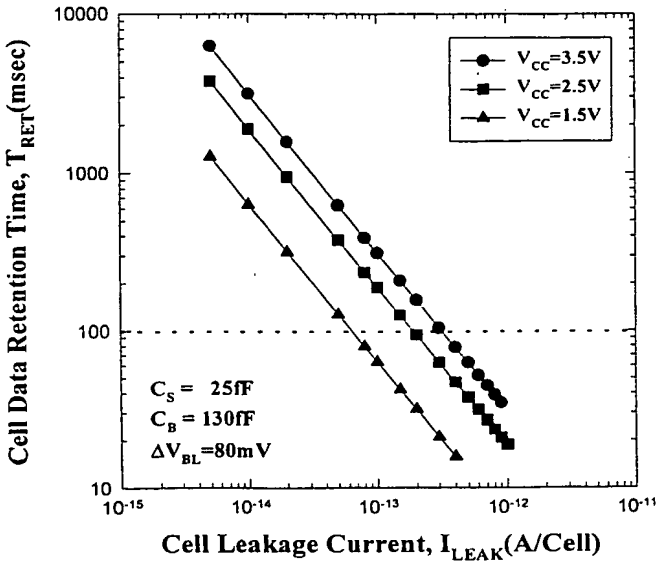


Fig. 4. Memory cell data retention time versus the leakage current at storage node with the operation voltage as a parameter.

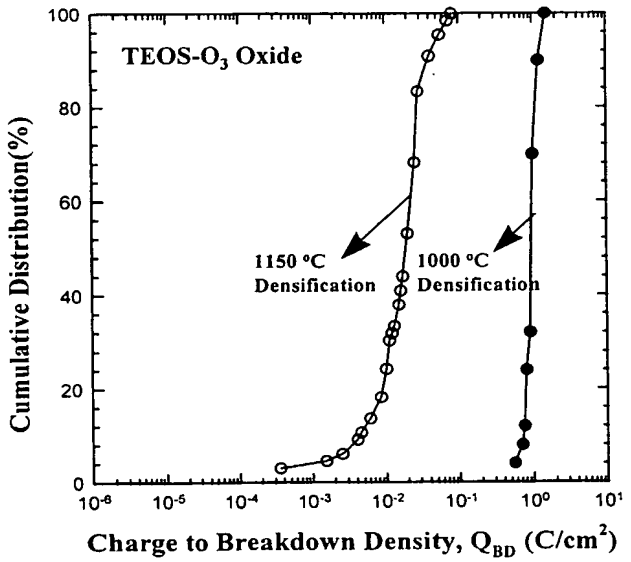
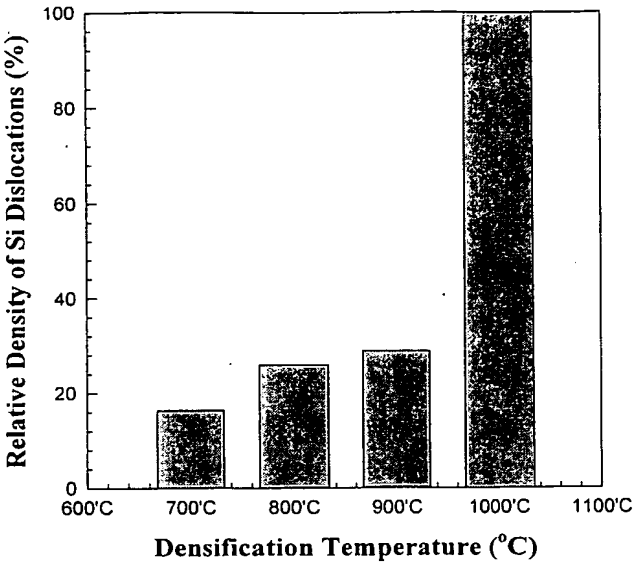


Fig. 5. Result of charge to breakdown density (Q_{BD}) measurement for different densification temperature of TEOS-O_3 oxide.



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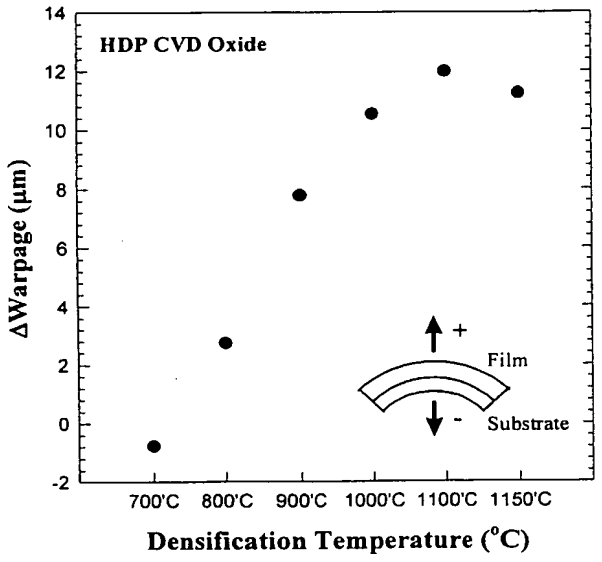


(b)

Fig. 6. (a) Normalized density of STI dislocations and (b) the wafer warpage for various densification temperatures of trench filling high-density plasma (HDP) oxide.

warpage and gate oxide degradation. Fig. 5 shows the result of charge-to-breakdown density (Q_{BD}) measurement for different densification temperature of TEOS-O_3 oxide using STI edge intensive test pattern. The gate oxide reliability was severely degraded for the high-temperature densification of TEOS-O_3 oxide. This result indicates that the gate oxide at the STI edge was degraded due to the stress, which was induced from the large volume shrinkage of TEOS-O_3 oxide at high-temperature densification. High-density plasma (HDP) oxide has advantages of the superior step coverage and the low etch-rate in HF solution even though the densification is applied at relatively low temperature [5]. In our experiment, the trench was filled with HDP oxide, followed by densification at the temperature ranging from 700 to 1000 °C. Fig. 6 shows the normalized density of STI dislocations and the wafer warpage for various densification temperatures of HDP oxide. The less STI dislocations were observed as the lower densification temperature was applied by virtue of the reduced mechanical stress [14].

It has been known that the crystal defects are strongly dependent on the implantation conditions (e.g., dopant species and dose) [10]. The different doses of arsenic and phosphorus were investigated for n^+ contact hole implantation. Fig. 7 shows the normalized density of STI dislocations for different implantation conditions. STI dislocations are decreased about 80% by implanting arsenic (2×10^{15} cm^{-2}) compared to

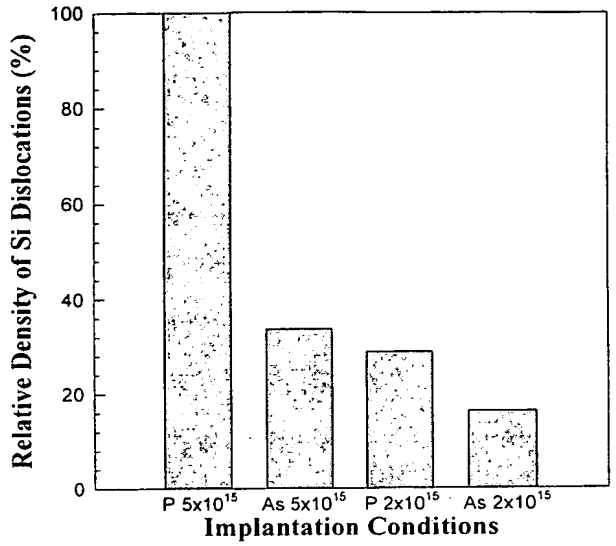


Fig. 7. Normalized density of STI dislocations for different implantation conditions.

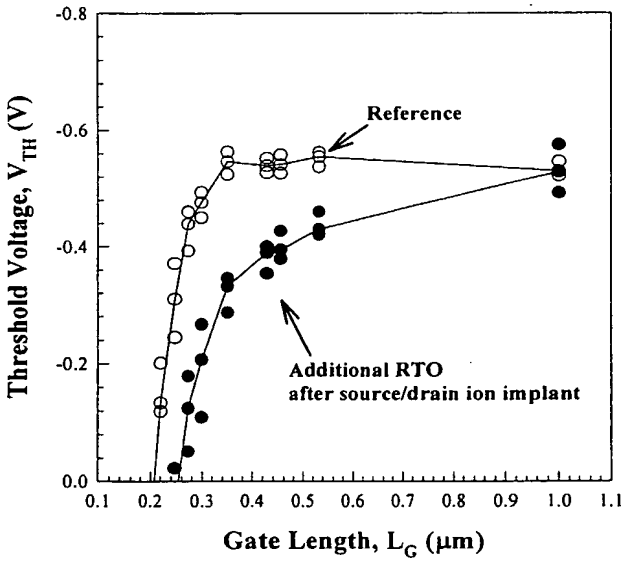
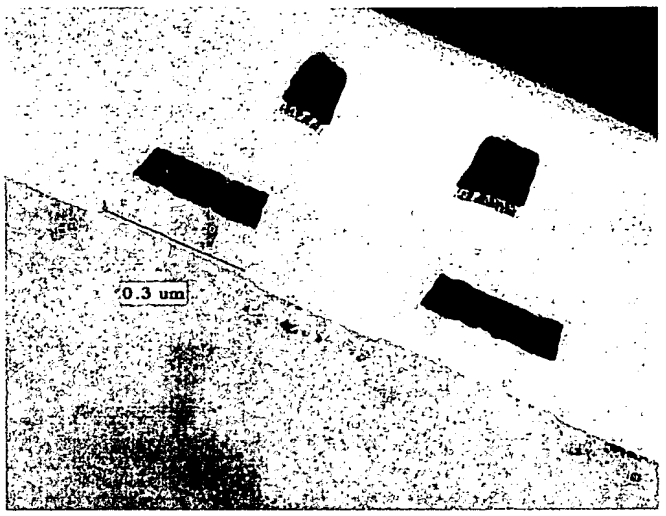


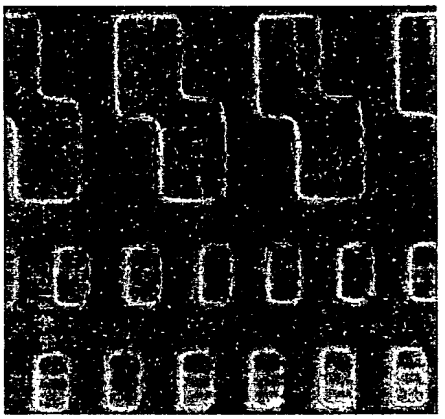
Fig. 8. Threshold voltage (V_{TH}) roll-off characteristics of buried channel PMOS. When the rapid thermal oxidation (RTO) was additionally adopted after source/drain implantation (filled circle), the short-channel effect of buried channel PMOS is significantly aggravated below 0.35 μm channel length due to the oxidation-enhanced boron diffusion.

phosphorus (5×10^{15} cm^{-2}). This result implies that the implantation of relatively higher dose and lighter ion produces more crystal defects which generate STI dislocations.

For the purpose of reducing the overall crystal defects before capacitor formation, it is necessary to cure the crystal defects from source/drain implantation. The rapid thermal oxidation (RTO) was additionally applied after source/drain implantation. STI dislocations were fully eliminated by the gettering effect of oxidation and no degradation of the junction characteristics was observed. However, the short-channel effect of buried channel PMOS was severely aggravated



(a)



(b)

Fig. 9. (a) Cross-sectional TEM and (b) the plan-view SEM images of STI dislocations when rapid thermal nitridation (RTN) was performed instead of gate reoxidation.

below 0.35 μm channel length due to the oxidation-enhanced boron diffusion, as depicted in Fig. 8. This result implies that the doping profiles of channel and source/drain of buried channel PMOS were indispensably redistributed during the additional RTO. In previous report [13], the activation energy of eliminating STI dislocations (5.0 eV) is larger than that of boron diffusion (3.46 eV). For high-density DRAM devices, therefore, it is not adequate to apply the heat treatment additionally after source/drain implantation for eliminating STI dislocations without the redistribution of boron.

As long as STI dislocations are located outside the depletion region, they could not have any detrimental effect on the pn junction characteristics. Therefore, STI dislocations are tried to be pinned at their generation site by relieving the cumulated mechanical stress before reacting with the crystal defects from source/drain implantation. The mechanical stress is induced during the gate formation; gate oxidation, gate poly doping ($POCl_3$), and so on. In order to relieve the cumulated mechanical stress before source/drain implantation,

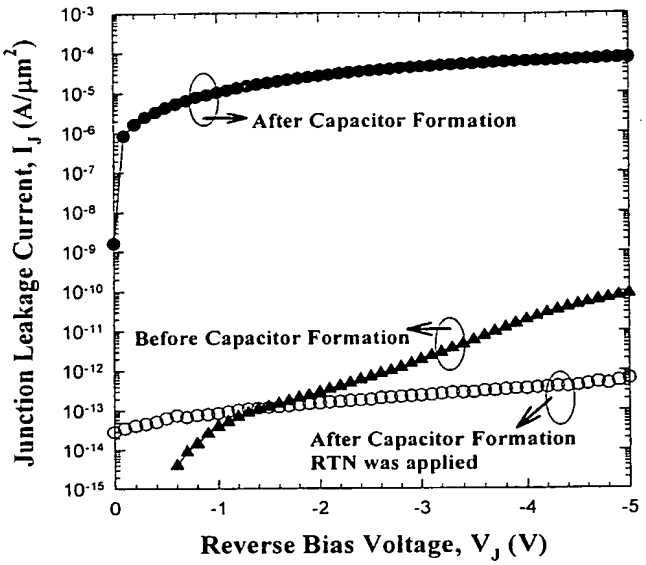
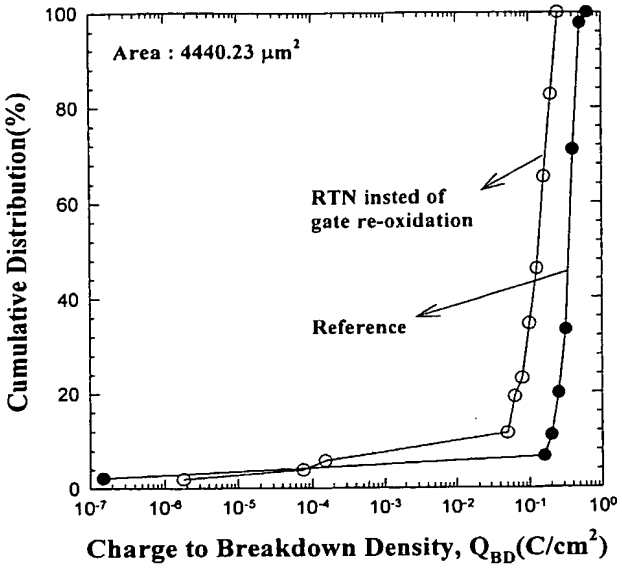


Fig. 10. Reverse-biased leakage current before (filled triangle), after (filled circle) capacitor formation and rapid thermal nitridation (RTN) was applied (open circle) measuring p^+-n junction in an actual sense amplifier (S/A).

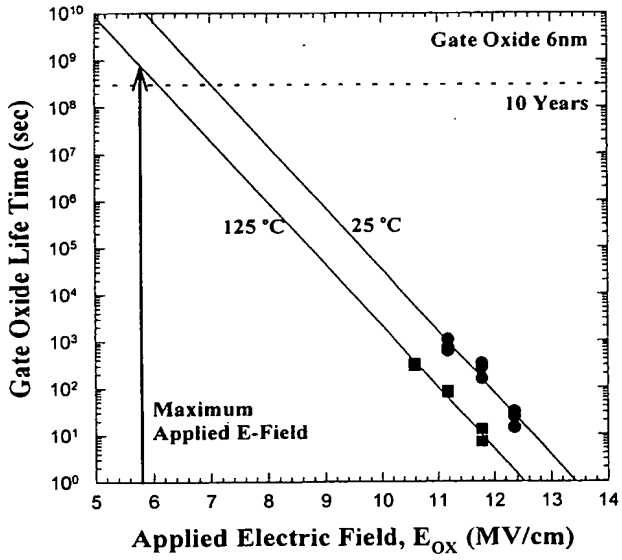
the rapid thermal nitridation (RTN) was performed instead of gate reoxidation. Fig. 9 shows (a) the cross-sectional TEM and (b) the plan-view SEM images of STI dislocations when RTN was applied. As depicted in Fig. 9(a), STI dislocations were located at the 0.075 μm depth. Fig. 9(b) shows that STI dislocations were eliminated at the Si surface. Since the junction depth of our device is about 0.12 μm, these results implies that STI dislocations were successfully pinned inside of the source/drain region. Fig. 10 shows the effect of gate reoxidation and RTN on the reverse-biased junction leakage current. When RTN was applied instead of gate reoxidation (open circle), good junction characteristics could be obtained. This result also indicates that STI dislocations could not penetrate the depletion region of pn junction. In order to investigate the gate oxide integrity, charge-to-breakdown density (Q_{BD}) and time-dependent-dielectric-breakdown (TDDB) were measured using the gate edge intensive test pattern, as depicted in Fig. 11. Although Q_{BD} was slightly lowered due to the relatively thinner gate oxide at the gate edge, the result of TDDB measurement indicates that the gate oxide could operate without suffering breakdown over ten years.

IV. Conclusions

When the crystal defects and the mechanical stress are combined under thermal annealing, STI dislocations are generated. An anomalous junction leakage current induced by STI dislocations considerably degrades the refresh characteristics and the standby current of DRAM device. STI dislocations are successfully clamped outside the depletion region of pn junction by judicious control of process-induced defects and mechanical stress. In this work, we have acquired the highly reliable performance of an experimental 16-Mb DRAM with the minimum feature size of 0.15 μm, and this technology can be fairly extensible to the future high-density DRAM devices.



(a)



(b)

Fig. 11. Results of (a) charge to breakdown density (Q_{BD}) and (b) time dependent dielectric breakdown (TDDB) measurement using the gate edge intensive test pattern.

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In 1983, he joined Samsung Electronics Company, Ltd., Kyungki-Do, Korea, where he has been involved in the development of DRAM's, ranging from 64 K to 1 Giga-bit densities. Currently, he is a Technical Director responsible for the research and development of future memory technology. He has been a Project Leader for the development of the world's first 1-Gb DRAM using 0.18-μm CMOS technologies from 1994 to 1996. His current major activity is focused on the development of technologies for low-power and high-performance multi-giga-bit density DRAM's. His research interests are memory device reliability, yield modeling on memory device, low-power sub-0.15-μm CMOS technology, memory cell technology, and multilevel metallization for high-performance of multi-giga bit DRAM's. He is interested in applying SOI technology into DRAM application, resulting in the successful development of a 16-Mb SOI DRAM, which is the highest density ever reported in 1994. He has published more than 45 technical papers on the field of memory technology. He holds 25 patents related to memory technology.

Dr. Kim received the grand prize of the Samsung Group twice for the successful development of 1-Mb DRAM and 1-Gb DRAM in 1986 and 1996, respectively. He is currently a Committee Member of the International Electron Device Meeting (IEDM) and the Korean Semiconductor Symposium (KSC).

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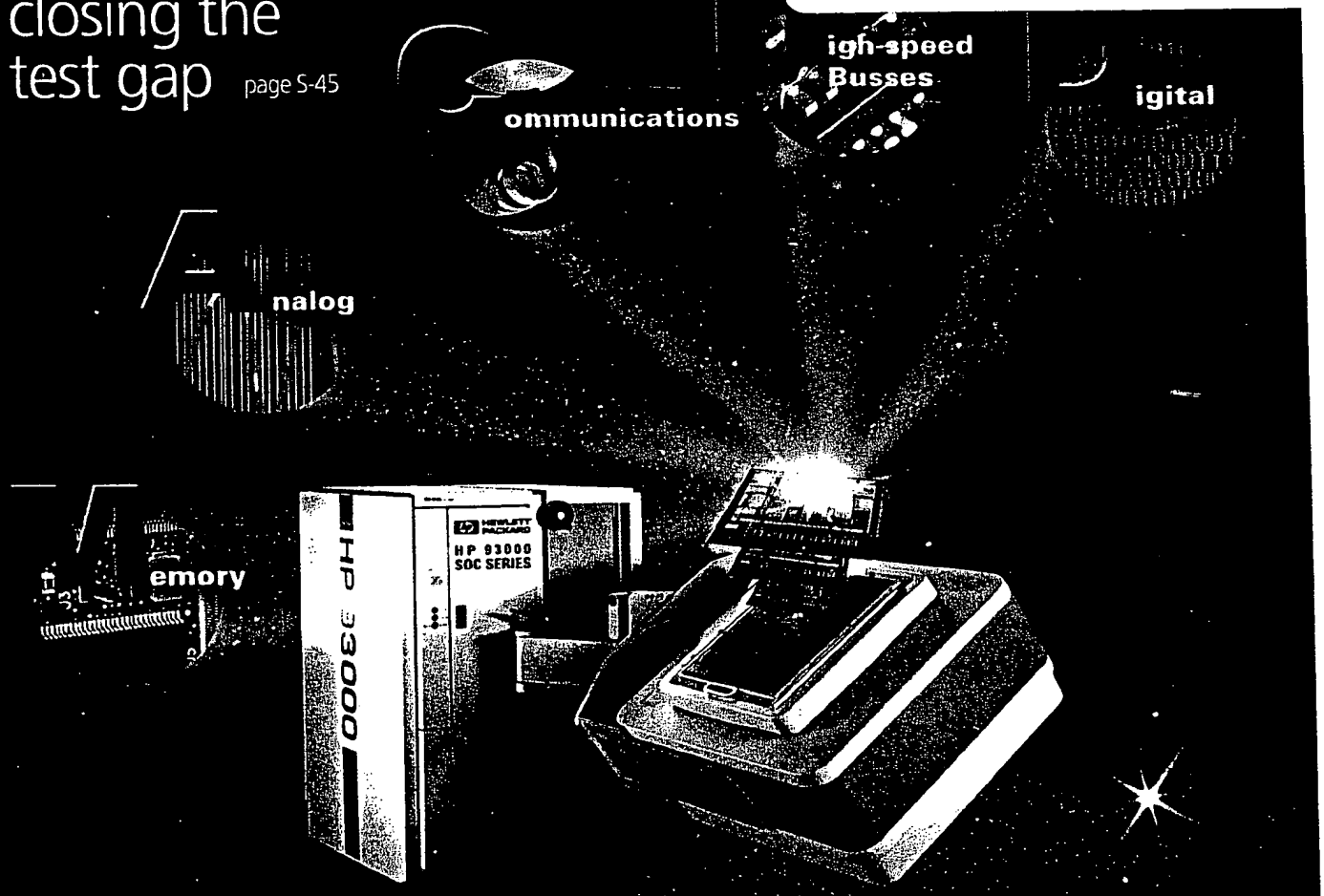
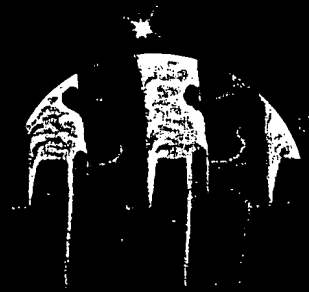
ESIGN ● PRODUCTION ● ASSEMBLY

System-on-a-Chip: closing the test gap

page S-45





Sub-0.18 µm damascene etch schemes

page 21

Country profile: French industry developments

page 17

Sub-0.18 µm STI by APCVD TEOS:Ozone

The applications lab of SVG Thermal Systems (formerly Watkins-Johnson Semiconductor Equipment Group) shows how linear-injected atmospheric-pressure CVD TEOS:O_3 can extend to shallow trench fill at 0.10 µm.

Trench isolation is now commonly used for most sub-0.35µm products. Leading-edge isolation trenches on the order of ~0.15-0.18 µm wide are currently used in production. Development evaluations targeting 0.13 µm and lower design rules are taking place now with structure widths to less than 0.10 µm. This reduction in trench width challenges the ability of the fill oxide process to meet the increasingly demanding technology node requirements, including void-free fill, uniform oxide characteristics across 200 and 300 mm substrates, at a reasonable cost of ownership (COO).

One technique that is meeting these challenges is the Linear Injected APCVD TEOS:O_3 process. This article focuses on the success of the APCVD TEOS:Ozone Linear Injector in meeting the technology requirements for sub-0.18 µm shallow trench isolation. Extension to the 0.10 µm generation, shallow trench fill capability, film characteristics, scaling to 300 mm, and comparisons to other trench fill processes are also presented.

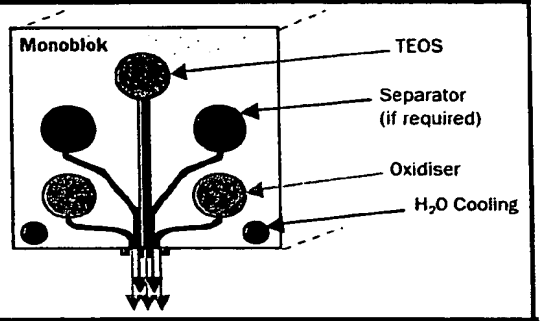
LINEAR INJECTOR DEPOSITION

Published studies of TEOS:Ozone reactions in the formation of SiO_2 deposition at or near atmospheric pressure indicate that intermediate species are formed in the gas phase. These intermediates first initiate then complete the SiO_2 film growth on the wafer surface [1-10].

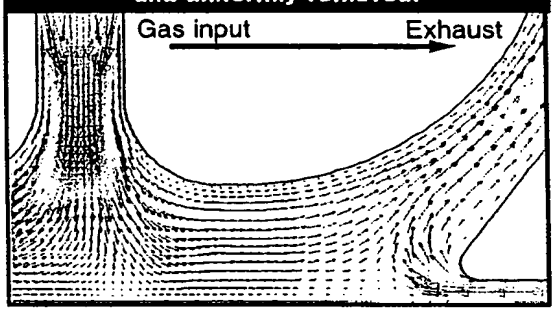
The gas-phase reactions also form parasitic species that can reduce deposition rate and chemical efficiency. They can also contribute to excessive formation of solids in the gas stream, leading to particles on or near the wafer surface. Shareef *et al* has reported that showerhead-type reactors in particular exhibit severe reduction in deposition rate as well as an increase in chamber powder formation occurring at deposition temperatures above 450°C [11]. This may be due to accelerated formation of parasitic species, since the gases are injected in a pre-mixed state and reach high temperatures well before reaching the wafer surface.

Higher-quality films have been reported to be produced at higher deposition temperatures [12]. Our tests confirm this for the regime from 400-500°C [6]. Higher deposition temperatures produce superior film quality, lower surface sensitivity and better gap fill. Therefore, the optimum reactor for depositing TEOS:Ozone would be one that simultaneously controls the gas-phase reactions to minimise parasitic species while allowing higher deposition temperatures to be used.

Linear injector.



Reaction by-products are quickly and uniformly removed.



An injection design which precisely controls the gas-phase reactions at high deposition temperatures is the Linear Injector (Figure 1). Reactant (TEOS) and oxidisers (O_2/Ozone) are injected in separate laminar curtains at high velocities from a water-cooled injector. These streams diffuse together as they flow to the wafer. The amount of mixing in the gas phase is controlled by the flow rates of the respective injected gases, which determine the stream velocities. The exhaust slot is near and parallel to the input curtain so the reaction by-products are quickly and uniformly removed (Figure 2). The bi-lateral and symmetrical exhaust path equally split the gas streams into two symmetrical deposition zones, each about 50 mm in width. The wafer is transported under the fixed gas stream so each area of the wafer receives the exact same gas mixture.

This control of the input gas mixture and temperature, and by-product removal provides a precisely controlled reaction process at the desired high deposition temperature.

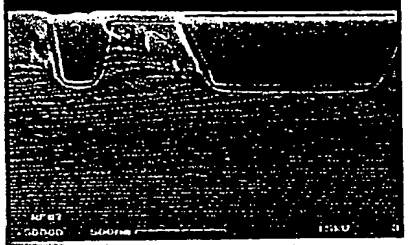
At 500°C, high deposition rate films (well over 3000Å/min) with high film qualities (etch rate <1.2x thermal oxide) and low particulate density (<six particles/wafer@0.20µm size) can be deposited with excellent gap fill. (These specifics will reported in a subsequent section.)

This linear design has been successfully scaled to larger size substrates such as 200 mm, 300 mm and even 400 mm. The injector length increases to accommodate the larger substrate, and advantageously the gas mixing and residence path do not change. This is a distinct advantage over pre-mix radial showerhead-type gas injection systems. ➤

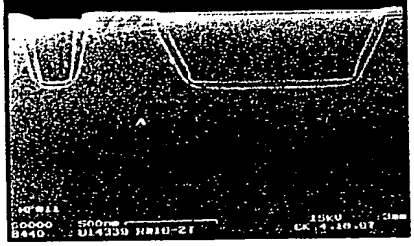
Table 1. Comparison of gas injection designs.

Design Feature	Linear Injector	Showerhead Injector
Deposition zone, scaling to 300 mm	Narrow and Linear, 50 mm wide, one independent of wafer size	Wider and radial, dependant on wafer size, centre to edge: 150 mm wafer - 75 mm 200 mm wafer - 100 mm 300 mm wafer - 150 mm
Gas port to exhaust relationship	Equal distance across wafers, consistent chemical residence	Varies from centre to edge, inconsistent chemical residence
Valve cycling over wafer?	None	Yes, can cause transients on product
Chemical mixing type	Separated chemical delivery, higher chemical efficiency	Pre-mix chemical, lower chemical efficiency

0.22 µm, 3:1 aspect ratio fill at 2470Å/min.



0.22 µm, 3:1 aspect ratio fill at 3470Å/min.



Technology node (CD) vs on-wafer specification requirements.

	0.15 µm	0.13 µm	0.10 µm
	4Gb	4Gb	16Gb
	<1% 1σ	<1% 1σ	<0.75% 1σ
	<0.13	<0.10	<0.06
	0.12 µm	0.10 µm	0.08 µm
	5.00E+09	2.00E+09	1.00E+09
			2 mm
	~70-100 nm	~50-80 nm	~40-60 nm
	~1000°C, 30 min	~1000°C, 30 min	~1000°C, 30 min

When these systems scale from 200 mm to 300 mm the residence path of the centrally delivered gas species increases by 50%. This is a common issue with plasma-based reactors, parallel-plate and HDP type, in which plasma density and gas distribution variations can directly impact the ability to deliver uniform film qualities, charge levels, and gap fill across these larger substrates. Table 1 summarises the design principles for both Linear Injection and showerhead-type injection.

0.15-0.10 µm SHALLOW TRENCH ISOLATION FILM REQUIREMENTS

The continued reduction of the critical dimensions on sub-0.18 µm technology increases demands on the isolation trench oxide film characteristics. Critical parameters include trench gap-fill capability, uniform gap fill across the wafer, film thickness uniformity, lower defect densities, lower metal content, and all measured with smaller edge exclusions (Table 2). All of these requirements must be met simultaneously, and with acceptable CoO. This is quite challenging to both equipment and process designers and to those development engineers that must evaluate the various deposition options.

Another important consideration is the breadth of the process window for the isolation trench fill. Natural and atypical variances do occur in the control systems of the various reactors and processes under consideration. Minimising the number of critical control systems and operating with a wide process window that can accommodate natural variances in these systems enhances the reliability of the process. In particular, gap fill, film stress, and film shrinkage must be minimally effected when control systems vary within their design tolerances.

ROBUST PROCESSING WITH LINEAR INJECTION

• *Gap-fill capability at high deposition rate*

The first and foremost critical requirement for the oxide fill process is to achieve complete void-free fill into the aggressive structures of the sub- 0.18 µm technologies. Additionally the ability to combine the complete gap fill with a robust high-deposition-rate, low-cost process is highly desirable. Figures 3 and 4 show complete gap fill and uniform planarisation post-CMP. These are 0.22 µm wide, 3:1 aspect ratio structures. Figure 3 was deposited at 2470Å/min; Figure 4 at 3740Å/min, an increase of 50%. This is a significant deposition rate increase and the process still provides excellent gap fill, as shown.

• *Etch rate, stress, shrinkage, gap fill, thickness uniformity at high deposition rates*

• *Etch rate*

Concern over degradation of other critical film properties such as etch rate and stress as an effect of the high-deposition-rate film are addressed in Figures 5-7.

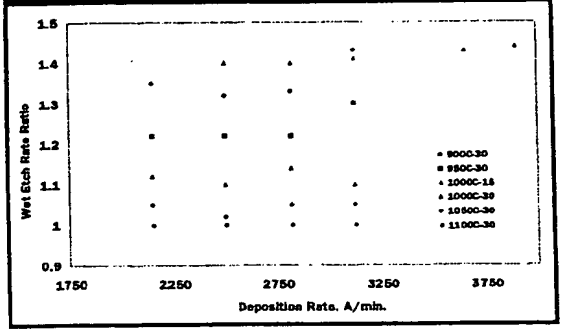
Figure 5 shows that the deposition rate has very little effect over wet etch rate ratio (30:1 BOE), even when deposition rate is increased by over 50%. Clearly densification temperature and time control the wet etch rate ratio independently of the deposition rate. The etch rate shows very well organised behaviour, with films densified at 1100°C showing the same etch rate as thermal oxide (1:1 etch rate ratio).

• *Film stress*

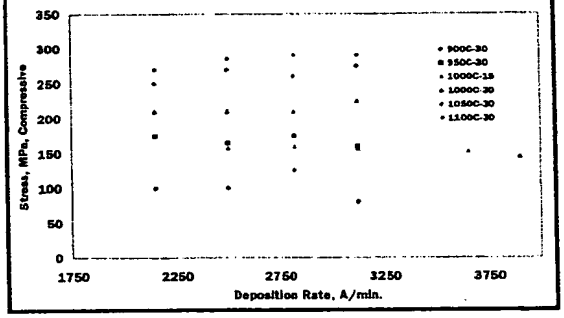
Film stress also shows the same relationship as wet etch rate ratio, the dense condition controls the stress independently of the deposition rate (see Figure 6).

Stress is also shown to vary slightly, depending on the specific deposition

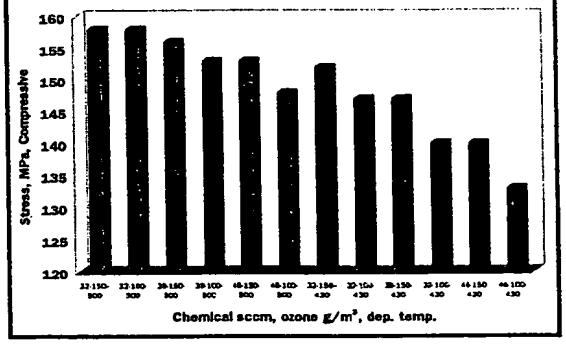
Wet etch rate as a function of the deposition rate, dense temperature and time. Wet etch rate is controlled by the dense conditions, not the deposition rate of the film.



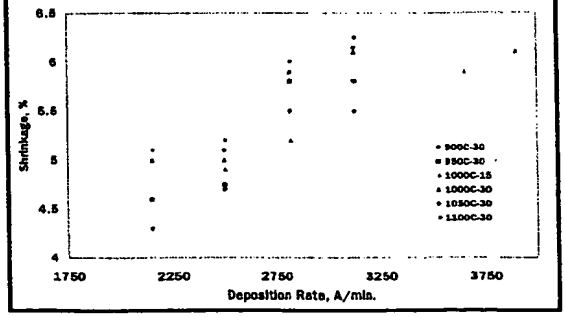
Stress as a function of the deposition rate, dense temperature, and time. Final film stress can be precisely controlled by the dense conditions. This can ease concern over design changes that may require a change in the film stress level.



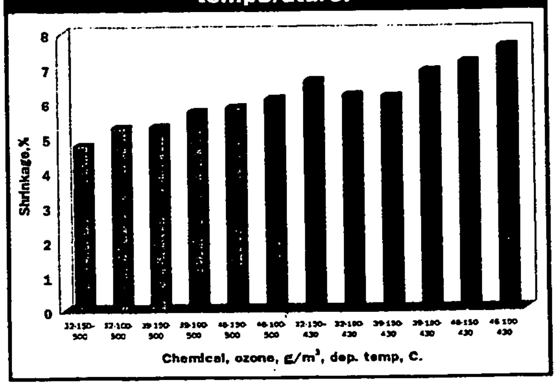
Post-dense stress versus chemical flow, ozone concentration, and deposition temperature.



Film shrinkage versus chemical flow, ozone concentration and deposition temperature.



Film shrinkage versus chemical flow, ozone concentration and deposition temperature.



conditions. Figure 7 details the effect of varying the chemical flow, ozone concentration and deposition temperature. This data is post-densification at 1000°C for 15 minutes in nitrogen. The general trends show that higher-temperature, higher-ozone, and lower-chemical-flow films exhibit higher compressive stress post-dense. The specific densification system ambient gas may not be 100% nitrogen, with O_2 and HCL common fraction additives.

• *Film Shrinkage*

Film shrinkage is only slightly effected by the deposition rate. Increasing the deposition rate by over 50% only increases the film shrinkage by 1-1.5% (see Figure 8).

Film shrinkage is also shown to vary slightly depending on the specific deposition conditions. Figure 9 details the effect of varying the chemical flow, ozone concentration, and deposition temperature. This data is post-densification at 1000°C for 15 minutes in nitrogen. The general trends show that higher-temperature, higher-ozone, and lower-chemical-flow films exhibit lower shrinkage.

• *Gap-fill extension to 0.10 µm technology*

Gap-fill extension capability to smaller geometries is critical in today's manufacturing and development environment. Table 3 shows data from 1998 indicating APCVD gap fill was superior to both HDP and SACVD, extending to 0.13 µm. Figure 10 shows the complete gap fill of a 0.10 µm generation trench by the Linear Injected TEOS:Ozone APCVD process.

• *Thickness uniformity*

Achieving high yields requires good thickness uniformity to ensure optimum across the wafer planarisation without dishing to the oxide or erosion to the nitride corners. The uniformity characteristics of the APCVD TEOS:Ozone process are shown in Figure 11. One-sigma uniformity of 1% can be considered complete satisfactory to the 0.13 µm generation, and approaches the requirement of 0.75% one-sigma for the 0.10 µm generation.

CONCLUSION

TEOS:Ozone processing is highly used for shallow trench isolation applications owing to its excellent gap-fill capability. We have reviewed the requirements for precise control of the complicated TEOS:Ozone reaction to produce a high-quality shallow trench oxide film. Special consideration to the gas injection system design is critical to obtain all of the desirable film properties simultaneously with a chemically efficient process. Data presented on stress, etch rate, shrinkage and uniformity all show that high (>3000Å/min) deposition rates can be used, and the final film properties are primarily and precisely controlled by the densification conditions. The requirements for the 0.10 µm generation - including gap fill - have been met by the Linear Injection APCVD TEOS:Ozone process. The benefits of the Linear Injector include short gas residence time, rapid exhausting of the gas-phase by-products, high chemical efficiency, and effortless scaling from 200 to 300 mm.

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Complete gap fill at 0.10 µm: 0.10 gap at pad oxide; 0.07 µm bottom gap; 0.52 µm depth; 86-88° sidewall angle; post-densification and etch decoration, 20 s in 30:1 BOE.

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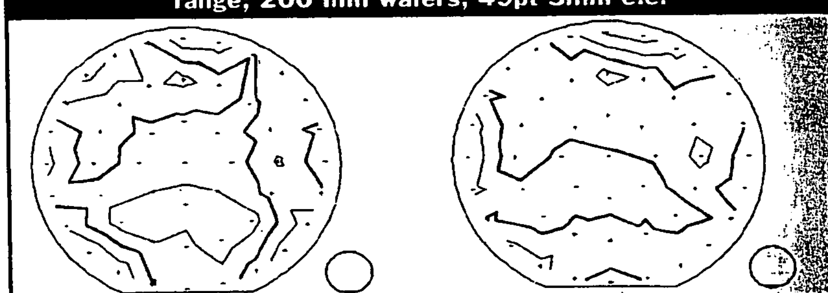
Thickness uniformtiy: 8000Å films; 1.0% 1σ; ±2.1% range; 200 mm wafers; 49pt 3mm e.e.



Comparison of gap-fill technologies (Nandakumar *et al* 1998 IEDM13).

Criteria	Concern	HDP	Gap-fill SACVD	[illegible]
Minimum void-free trench gap-fill	[illegible] poly wrap-around	[illegible]	[illegible]	[illegible]
Densification required	[illegible]	Yes	Yes	[illegible]
Film shrinkage %	Delamination, [illegible]-induced defect	[illegible]	[illegible]	[illegible]
Step-height uniformity	STI corner, gate oxide integrity	Good	Poor	[illegible]